MODEL DQ130

MAGNETIC TAPE COUPLER
INSTRUCTION MANUAL

B 922.411

FORWARD

SECTIONS 1-4 of this Instruction Manual are intended to assist an operator in installing and operating a magnetic tape subsystem which includes a Distributed Logic Corporation magnetic tape coupler. The material assumes a knowledge of the instruction set and operating programs for the PDP-11 computer, specifically those programs directly applicable to the LSI-11, 11/2, and 11/23 computer family.

SECTION 5 contains a Theory of Operation. Section 6 contains Detailed Logic Drawings, and a Troubleshooting Guide. A second companion document entitled "Software Aids And Diagnostic" contains operating instructions and a listing for the DILOG-supplied diagnostic.

Prior to reading this guide, the user should become thoroughly familiar with the LSI-11 based hardware/software combination he is using, and be certain he has read the manuals on the tape formatter and transports with which the coupler is to be used.

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TABLE OF CONTENTS

SECTION	TITLE	PAGE
1.	GENERAL DESCRIPTION	
1.0	Introduction	1-1
1.1	General Description.	1-2
1.1.1	LSI-11 Q Bus Interface	1-5
1.1.2	Interrupt	1-5
1.1.3	Tape Interface	1-5
1.2	Specifications	1-11
2.	INSTALLATION	
2.0	Introduction	2-1
2.1	Pre-Installation Checks.	2-1
2.2	Configuration.	2-2
2.3	Installing	2-4
3.	OPERATION	
3.0	Introduction	3-1
3.1	Tape Format.	3-2
3.2	Booting From Magnetic Tapes.	3-2
3.3	Streaming Tape	3-2
4.	PROGRAMMING	
4.1	Programming Definitions.	4-1
4.2	Tape Coupler Functions and Registers	4-1
4.2.1	Status Register (MTS).	4-3
4.2.2	Command Register (MTC)	4-5
4.2.3	Byte Record Counter (MTBRC).	4-6
4.2.4	Current Memory Address Register (MTCMA).	4-7
4.2.5	Data Buffer (MTD).	4-7
4.2.6	Tape Read Lines (MTRD)	4-8
4.2.7	Timer.	4-8
5.	TECHNICAL DESCRIPTION	
5.0	Introduction	5-1
5.1	General Description.	5-1
5.1.1	Computer Interface	5-3
5.1.2	Microprocessor	5-3
5.1.3	Peripheral Interface	5-4
5.2	Functional Description	5-4
5.2.1	Computer Interface	5-4
5.2.1.1	Data/Address Receivers	5-6
6.	TROUBLESHOOTING GUIDE	
6.0	Introduction	
6.1	General	
6.2	Operating Precautions	
6.3	Possible Troubles	

TABLE OF CONTENTS, continued.....

SECTION	TITLE	PAGE
5.2.1.2	Control Receiver/Drivers.	.5-6
5.2.1.3	Data/Address Drivers	.5-6
5.2.2.4	Bus and Arbitration Sequence (State Processor). . .	.5-6
5.2.1.5	Bus Transfer Timing	.5-7
5.2.2	Microprocessor.	.5-10
5.2.2.1	Micro Data File	.5-10
5.2.2.2	Micro Data File Addressing.	.5-15
5.2.2.3	Micro Data File Multiplexer	.5-15
5.2.2.4	2901A Array and Status Register	.5-16
5.2.2.5	Control Memory and Register	.5-17
5.2.2.6	Control Store Address Programmer.	.5-17
5.2.2.7	D Bus Multiplexer	.5-19
5.2.3	Peripheral Interface.	.5-20
5.2.3.1	Peripheral Input Output Registers	.5-20
6.	TROUBLESHOOTING GUIDE	
6.0	Introduction.	.6-1
6.1	General	.6-1
6.2	Operating Precautions	.6-2
6.3	Possible Troubles	.6-2
APPENDIX A	CABLE LIST.	.A-1
APPENDIX B	GLOSSARY OF TERMS	.B-1

LIST OF TABLES

TABLE	TITLE	PAGE
1-1	Coupler/Q Bus Interface Lines.	1-6
1-2a	Coupler to Formatter Interface Lines J1.	1-8
1-2b	Coupler to Formatter Interface Lines J2.	1-9
5-1	Coupler Buses.	5-14
5-2	Coupler Register Storage	5-14
5-3	Control Inputs to 2901A	5-16
5-4	Status Register Bits	5-16
5-5	Address Modification Conditions.	5-19
5-6	Information Sources to D Bus	5-19
6-1	Troubleshooting.	6-3

LIST OF FIGURES

FIGURE	TITLE	PAGE
1-1a	Tape System (Maximum Configuration) Embedded formatter Tape Drives	1-3
1-1b	Tape System (Maximum Configuration) Stand Alone Formatter Tape Drives.	1-4
1-2	Coupler Board Configuration.	1-10
2-1	Backplane Configurations	2-3
4-1	Coupler Register Configuration	4-2
5-1	Simplified Block Diagram Tape Coupler.	5-2
5-2	Detailed Block Diagram	5-5
5-3	DATI - Slave, Q Bus.	5-8
5-4	DATO - Slave, Q Bus Transfers.	5-9
5-5	DATI - Q Bus DMA Transfers	5-11
5-6	DATO - Q Bus DMA Timing.	5-12
5-7	Interrupt Sequence Timing.	5-13
5-8	Microinstruction Word.	5-19

SECTION 1

GENERAL DESCRIPTION

1.0 INTRODUCTION

This material defines the functional characteristics of the Model DQ130 magnetic tape coupler which, when used with any industry standard formatted magnetic tape drive, comprises a complete LSI-11 compatible 9 track magnetic tape subsystem. Magnetic tape drives from manufacturers other than DEC can be used while still retaining software and format compatibility with the DEC TM-11 tape system. The Model DQ130 is completely contained on one quad module that occupies two device locations in the backplane. Data transfers are via the DMA facility of the LSI-11. Transfer rates vary, depending upon the density and speed of the drives included in the system, between 10,000 and 200,000 characters per second.

Up to two embedded-formatter tape drives or external stand-alone tape formatters may be connected to the Model DQ130. Each embedded-formatter tape drive is capable of handling an additional three slave drives. All industry standard external stand alone formatters are capable of handling four drives. The Model DQ130 can accommodate up to eight drives.

The optimal usage of the Model DQ130 is in situations where 9 track, dual density, 800/1600 bpi tape recording capabilities are required; however the Model DQ130 is compatible with single density 800 or 1600 bpi embedded-formatter tape drives or stand alone external formatters. In cases where single density 800 bpi NRZI format is the only density required, the Model DQ120 magnetic tape coupler should be considered.

The primary functions of the Model DQ130 coupler in a magnetic tape subsystem are to buffer and interlock data and status transfers between the computer I/O bus and the tape formatter, and to translate CPU commands into tape formatter control signals such as START, STOP, REWIND, GENERATE IR GAP, GENERATE EOF GAP, etc. The primary function of the formatter, is to control tape motion, establish data format, and perform error checking. The overall tape control function is a combination of the coupler functions which are related to the LSI-11 and the formatter functions which are related to the tape drives.

A microprocessor is the sequence and timing center of the coupler. The control information is stored as firmware instructions in Read Only Memory (ROM) on the coupler board. One section of the ROM contains a diagnostic program that tests the functional operation of the coupler. This self test is performed automatically each time power is applied or whenever an INIT command is issued on the CPU I/O bus. A green diagnostic indicator on the board lights if self test passes. If self test fails, the coupler has an automatic data protect feature that stops the CPU from interacting with the tape formatter and thus prevents writing erroneous information into critical data base areas.

Two additional indicators on the coupler board display dynamic operating conditions to an operator. The conditions displayed are Coupler Busy and Coupler Transferring Data (DMA Busy).

The coupler is connected to a tape formatter via a ribbon cable which plugs into two 50-pin 3M connectors located near the top at the center of the coupler.

1.1 General Description

The DQ130 magnetic tape coupler links an LSI-11 based computer to one or two tape formatters (embedded or stand alone). The formatter permits information to be read and written on tape between the LSI-11 system and other computers, either small or large scale, and of various manufacturers (DEC, IBM, Data General, Honeywell, etc.). The coupler performs the following major functions:

a. Buffers and interlocks data and status transfers across the computer I/O bus.

b. Translates computer command words into single commands or strings of commands to the tape formatter.

The formatter in a system performs the following major functions:

a. Controls the timing and the format of data transfers to the tape units.

b. Monitors the status of the tape units and the quality of the data transferred onto the tape and presents this information to the coupler.

c. Generates all discrete control signals to the tape units.

Each formatter can link up to four tape units to the computer in various configurations. Figure 1-1a illustrates a simplified system using embedding-formatter tape transports, and Figure 1-1b a system using stand along formatters.

A high-speed microprocessor is the control and timing center of the coupler. PROMs on the coupler board provide control instructions for the microprocessor, contain configuration-control information, and serve as general purpose logic elements. The microprocessor also permits an automatic self test of the coupler.

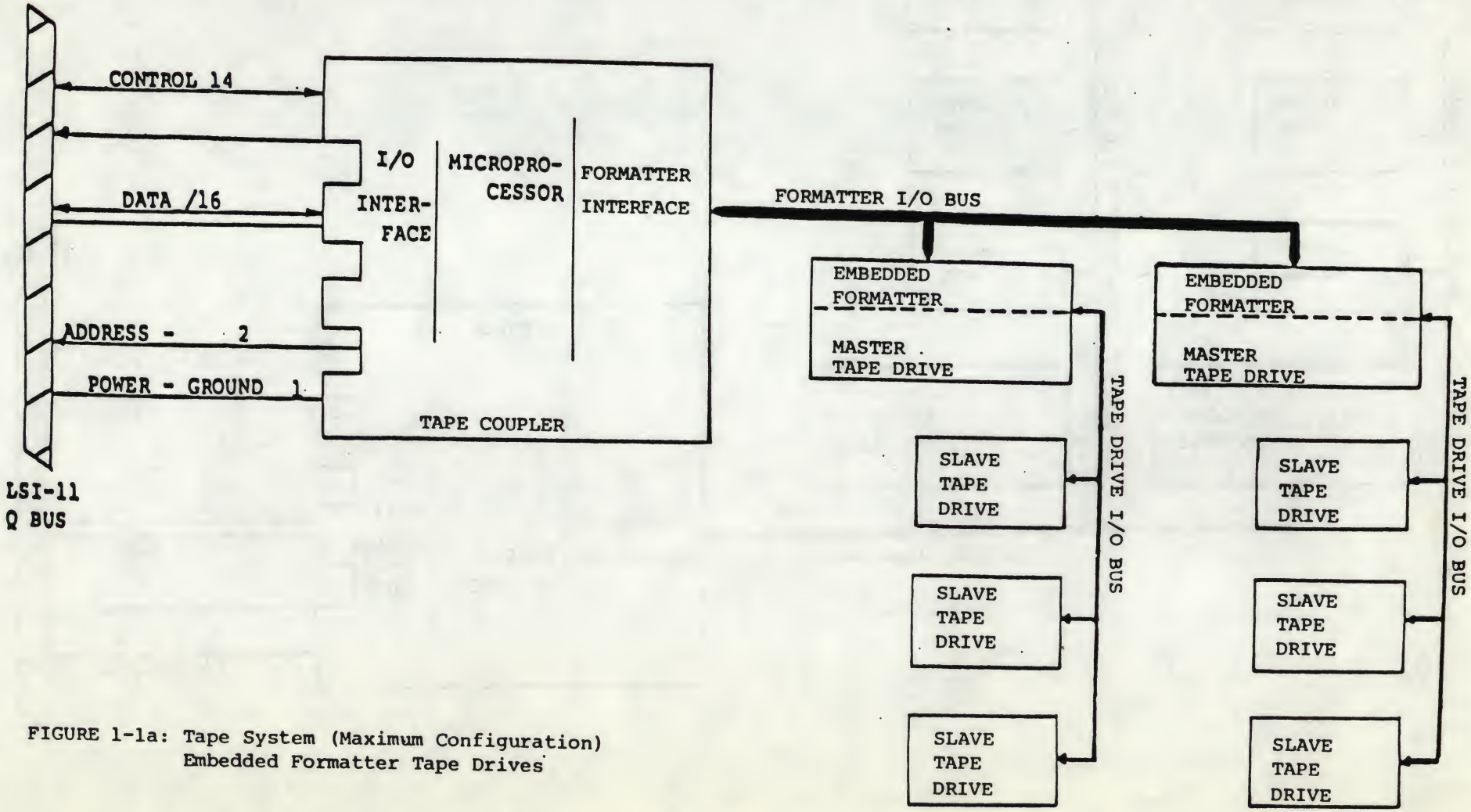


FIGURE 1-1a: Tape System (Maximum Configuration)
Embedded Formatter Tape Drives

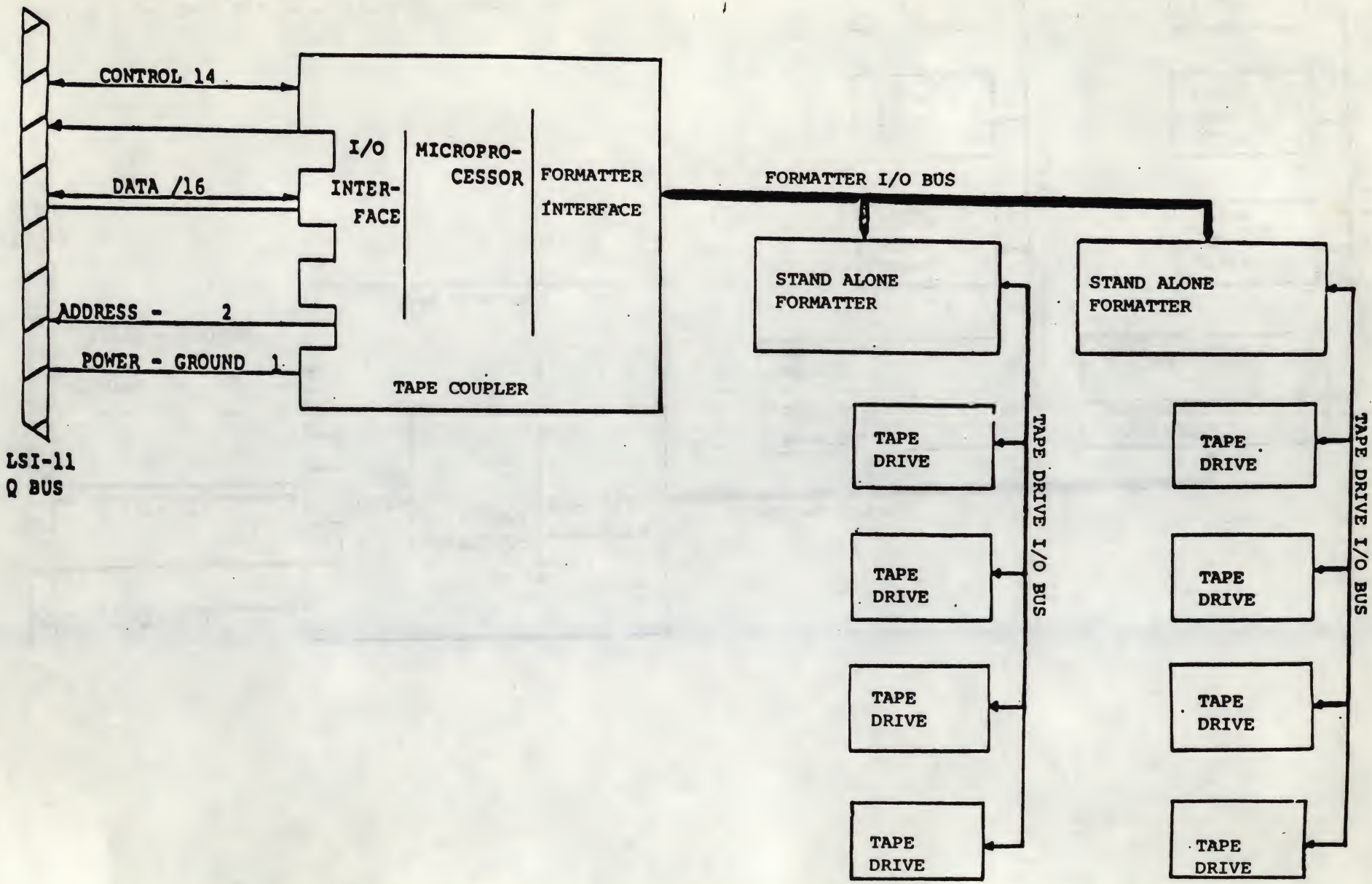


FIGURE 1-1b: Tape System (Maximum Configuration) Stand Alone Formatter With Tape Drives.

1.1.1 LSI-11 Q Bus Interface

Commands, data, and status transfers between the coupler and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O interrupt control. Data transfer rates are from 5,000 to 100,000 16-bit words per second, depending upon tape packing density and tape drive speed. Coupler/Q bus interface lines are listed in Table 1-1.

1.1.2 Interrupt

The interrupt vector address is factory set to address 224, which is compatible with TM-11 software. Interrupts are generated when processor attention is required or when an error occurs.

1.1.3 Formatter Interface

The coupler interfaces with the tape formatter through two 50-pin 3M connectors at the top, center of the coupler board. Two formatters are connected to the coupler in a daisy-chain manner. The maximum cable length from the coupler to the last formatter in a string is 25 feet. Coupler to formatter interface lines are listed in Table 1-2.

TABLE 1-1 Coupler/Qbus Interface Lines

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AJ1,AM1, RT1	GND		Signal Ground and DC Return
AN1	BDMR L	To	Direct Memory Access (DMA) request from controller: Active low
AP1	BHALT L	To	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	From	Memory Refresh. Not used.
BA1	BDCOK H	From	DC Power OK. All DC voltages are normal.
BB1	BPOK H	From	Primary power OK. When low activates power fail trap sequence.
BJ1,BM1,BT1,BC2	GND		Signal Ground and DC return.
BN1	BSACK L	To	Select acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	To	External Event Interrupt Request. Not used.
BV1,AA2,BA2	+5	From	+5 volt system power.
AD2,BD2	+12	From	+12 volt system power.
AE2	BDOUT L	From/To	Data out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	From/To	Reply from slave to BDOUT BDIN and during IAK.
AH2	BDIN L	From/To	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNCL	From/To	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	From/To	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	B1RQ L	To	Interrupt Request
AM2 AN2	B1AK1 L B1AK0 L	From/To	Serial interrupt acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain.
AP2	BBS7 L	From/To	Bank 7 select. Asserted by bus master when addresses in upper 4K bank (28-32K words) are placed on the bus
AR2 AS2	BDMG1 L BDMGO L	From/To	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.

(more)

TABLE 1-1 Coupler/Qbus Interface Lines, continued

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AT2	BINIT L	From	Initialize. Clears devices on I/O bus
AU2,AV2	BDAL0/DAL1	From/To	Data/address lines 0 & 1, (2 of 16)
BE2,BF2,BH2	BDAL2	From/To	Data/address lines, 2-15, (14 of 16)
BJ2,BK2,BL2	through		
BM2,BN2,BP2	BDAL 15		
BR2,BS2,BT2			
BU2,BV2			
AC1	BAD16	To	Extended Address Bit
AD1	BAD17	To	

TABLE 1-2A: COUPLER TO FORMATTER INTERFACE LINES

Coupler Connector J2 to P4 (Cipher, Pertec) to J124 (Tandberg, CDC) to JC (Digi-Data), to P1 (Cipher F880), to J1 (Kennedy 6809)

J2 SIGNAL	J2 GROUND	MNENONIC	DESCRIPTION
2	1	FFBY	Formatter Busy
4	3	FLWD	Last Word
6	5	DWD4	Write Data 4
8	7	FGO	Initiate Command
10	9	FWDO	Write Data 0
12	11	FWD1	Write Data 1
14	13	FSGL	Not Used
16	15	FLOL	Load on Line
18	17	FREV	Reverse/Forward
20	19	FREW	Rewind
22	21	FWDP	Not Used
24	23	FWD7	Write Data 7
26	25	FWD3	Write Data 3
28	27	FWD6	Write Data 6
30	29	FWD2	Write Data 2
32	31	FWD5	Write Data 5
34	33	FWRT	Write/Read
36	35	FRTH2	Read Threshold 2
38	37	FEDIT	EDIT
40	39	FERASE	Erase
42	41	FWFM	Write File Mark
44	43	FRTH1	Read Threshold 1
45*		FPAR	Parity Select
46	45	FTADO	Transport Address 0
48	47	FRD2	Read Data 2
50	49	FRD3	Read Data 3

*Grounded except when working with 7 track formatter

TABLE 1-2B: COUPLER TO FORMATTER INTERFACE LINES

Coupler J1 to P5 (Pertec, Cipher) to J125 (Tandberg, CDC)to JD (Digi-Data), to P2 (F880) to J2 (Kennedy 6809)

J1 SIGNAL	J1 GROUND	MNEMONIC	DESCRIPTION
1		FRDP	Read Data Parity
2		FRDO	Read Data 0
3		FRD1	Read Data 1
4		FLDP	Loan Point
6	5	FRD4	Read Data 4
8	7	FRD7	Read Data 7
10	9	FRD6	Read Data 5
12	11	FHER	Hard Error
14	13	FFMK	File Mark
16	15	FCCG/ID	CCG/IDENT
18	17	FFEN	Formatter Enable
20	19	FRD5	Read Data 5
22	21	FEOT	End of Tape
24	23	FOFL	Off Line
26	25*	FNRZ	NRZI
25*		F7TR	7 Track
28	27		Ready
30	29	FRWD	Rewinding
32		FFPT	File Protect
34	33	FRSTR	Read Strobe
36	35	FDWDS	Demand Write Data Strobe
38	37	FDBY	Data Busy
40	39	FSPEED	Speed
42	41	FCER	Corrected Error
44	43	FONL	On-Line
46	45	FTAD1	Transport Address 1
48	47	FFAD	Formatter Address
50	49	FDEN	Density Select

*Grounded except for 7 track formatter

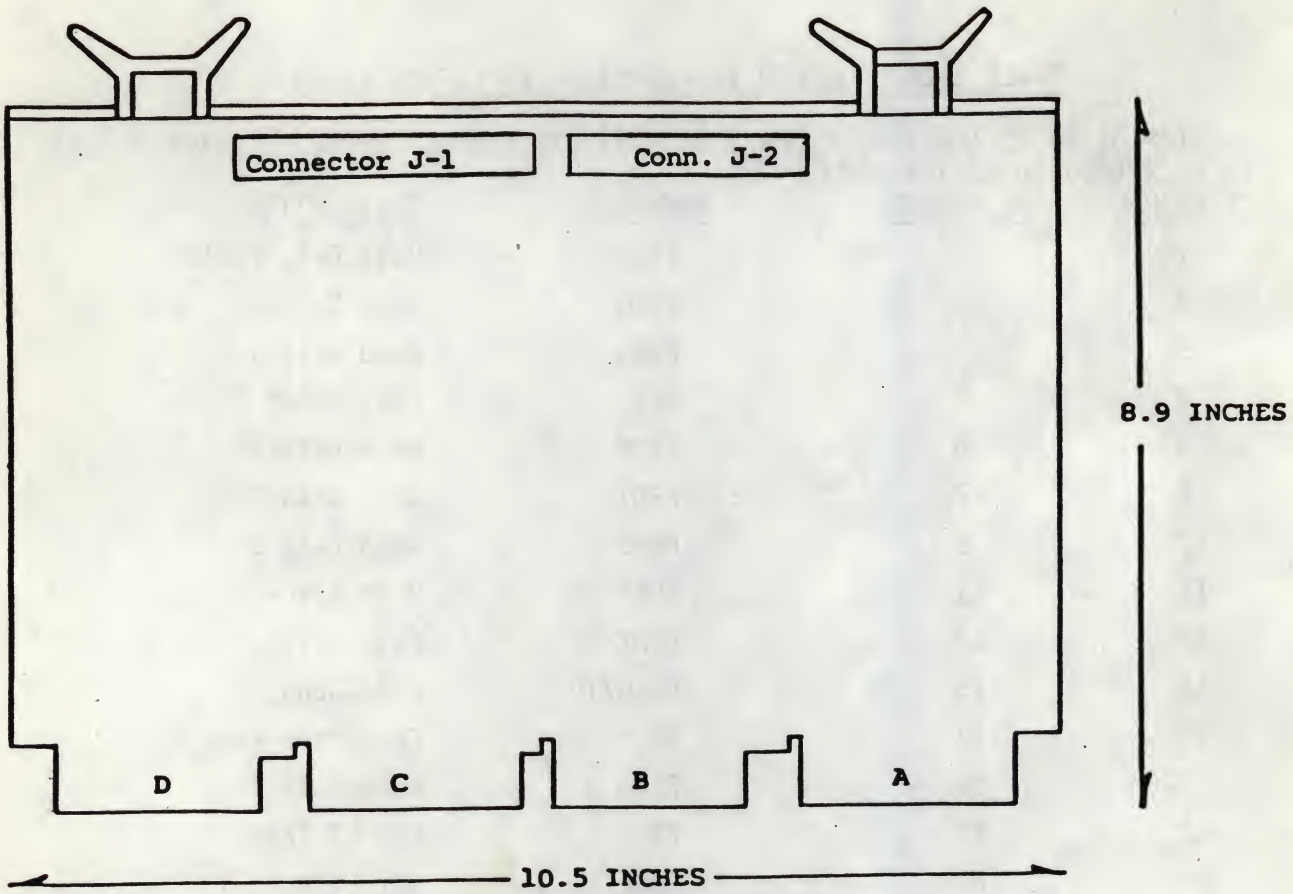


FIGURE 1-2: Coupler Board Configuration

1.2 Tape System General Specifications

DATA FORMAT

Industry standard non-return-to-zero (NRZ) or Phase Encoded (PE) recording.

9 tracks

Recording densities:
800 characters per inch
1600 characters per inch
800/1600 characters per inch

Interrecord gap 0.60 inch min.

Tape parity marks: LPC, CRC, LRC

MEDIA CHARACTERISTICS

TYPE

½" wide mylar base, oxide coated, magnetic tape.

REEL SIZE

7", 8½", or 10½" diameter tape reels containing 600, 1,200 and 2,400 feet of tape respectively.

DATA CAPACITY (megabytes)

Assumes approximate 80% recording efficiency:

		800 CPI	1600 CPI
600 Ft.	=	5.75	11.5
1,200 Ft.	=	11.5	23.0
2,400 Ft.	=	22.0	44.0

DATA TRANSFER RATE (Characters/Second)

		800 CPI	1600 CPI
12.5 ips	=	10,000	20,000
25.0 ips	=	20,000	40,000
37.5 ips	=	30,000	60,000
45.0 ips	=	36,000	72,000
75.0 ips	=	60,000	120,000
125.0 ips	=	100,000	200,000

REGISTER ADDRESS

Status (MTS) 772 520
Command (MTC) 772 522
Byte Record Counter (MTBRC) 772 524
Current Memory Address (MTCMA) 772 526
Data Buffer (MTD) 772 530
Tape Read Lines (MTRD) 772 532

COMPUTER I/O INTFC.

Interrupt Vector Address 224. DMA data transfer. 1 bus load.

COUPLER/FORMATTER INTERFACE	Coupler is compatible with formatters manufactured by Pertec, Kennedy, Tandberg, Cipher, CDC, Digi-Data.
PACKAGING	The coupler is completely contained on one quad module 10.44 inches wide by 8.88 inches deep.
DOCUMENTATION	One Instruction Manual is supplied with the coupler.
SOFTWARE	One diagnostic routine with object listing is supplied with a coupler (or the first of a series of couplers).
POWER	+5, ±0.25 VDC at 3.6 amps, from computer backplane.
ENVIRONMENT	Operating temperature 50°F to 140°F* Operating humidity 0% to 90% non-condensing.*

*NOTE: The quality of recording and reading information on magnetic tape is affected by temperature and humidity. The area where the tape is used should be maintained within the following limits:

Temperature: 15°C to 32°C
Humidity: 20% to 80%

SHIPPING WEIGHT 5 pounds including documentation.

SECTION 2

INSTALLATION

2.0 INTRODUCTION

The padded shipping carton that contains the coupler board also contains an instruction manual and a cable set to the first formatter. The coupler is completely contained on the quad-size printed circuit board. The formatter and/or tape drive, if supplied, is shipped in a separate carton.

CAUTION: IF DAMAGE TO ANY OF THE COMPONENTS IS NOTED, DO NOT INSTALL! IMMEDIATELY INFORM THE CARRIER AND DILOG.

Installation instructions for the formatter and/or tape drive are contained in the formatter or tape manuals.

2.1 Pre-Installation Checks

Many LSI-11 configurations were installed before DEC made a DMA device available for the PDP11/03 systems. Certain configurations require minor modifications before operating the DQ130 tape system. The modifications are as follows:

a. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the DQ130 coupler if the DMA refresh logic on the REV11-C is enabled.

b. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board), and add a jumper between pin 12 and pin 13 of D30.

c. In the case of a KD11-F board, if the 4K memory is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

d. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

e. If system requires more than a 4 x 4 backplane, place the REV-11 terminator in the last available location in the last backplane.

2.2 Configuration

To install the coupler module, proceed as follows:

CAUTION: REMOVE DC POWER FROM MOUNTING ASSEMBLY BEFORE INSERTING OR REMOVING COUPLER MODULE!

BE SURE THE COUPLER IS INSTALLED WITH THE COMPONENT SIDE UP OR FORWARD!

DAMAGE TO THE BACKPLANE ASSEMBLY MAY OCCUR IF THE COUPLER MODULE IS PLUGGED IN BACKWARDS!

1. Select the backplane location into which the coupler is to be inserted. The preferred location for the coupler is as the highest priority DMA device in the computer except for the disc controller, except if the DMA refresh/bootstrap ROM option module is installed in the system. The highest priority device is the device closest to the processor module. (Refer to Fig. 2-1)

   There are several backplane assemblies depending on the type system: H9270 backplane, DDV11-B backplane, BA11 expansion box, etc. Figure 2-1 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane, or the first location in the first backplane of multiple backplane systems.

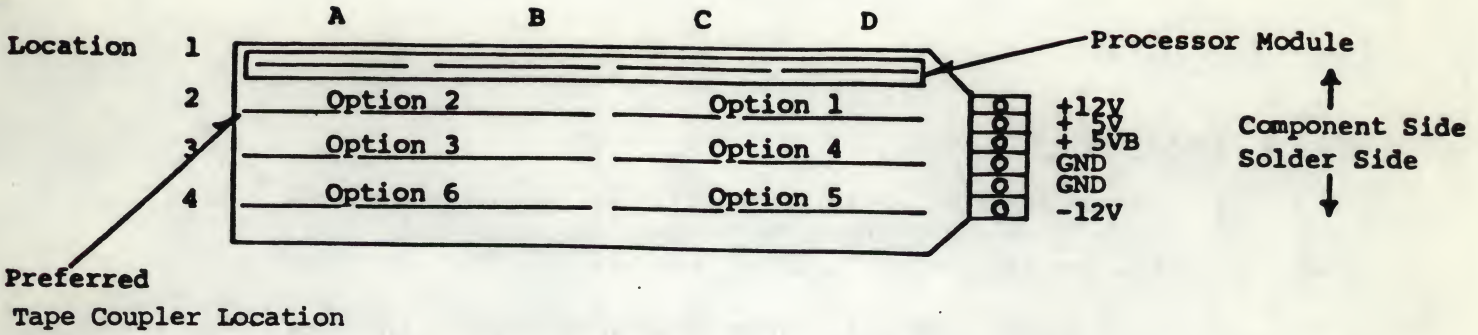
   Note that memory need not be installed next to the processor module; it is not DMA or interrupt priority dependent.

   It is important that all option slots between the processor and the tape coupler are filled if the coupler cannot be next to the processor. This is necessary to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signals are complete to the coupler slots. If empty slots exist between the coupler and any option board, the following backplane jumpers must be installed:

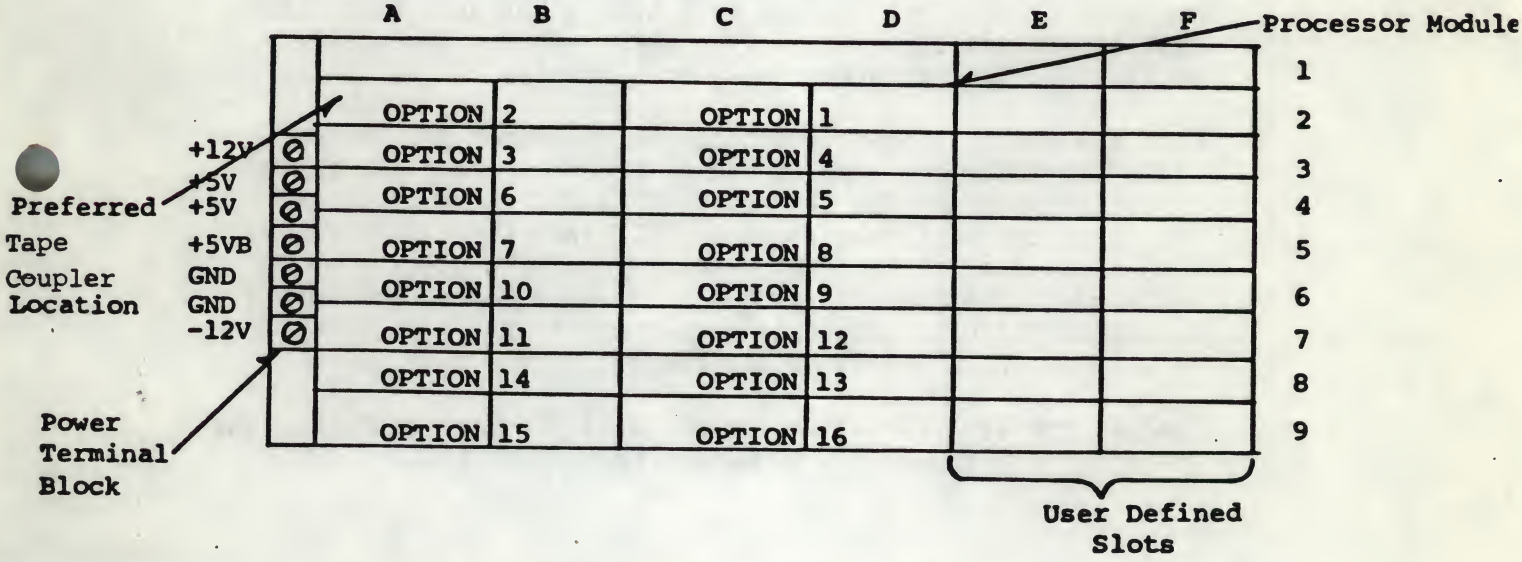
FROM	TO	SIGNAL
$\overline{\text{COXN2}}$	$\overline{\text{COXM2}}$	BIAK1/LO
COXS2	COXR2	BDMG1/LO

2. If a streamer type tape transport is to be used, cut the etch on the bottom side of the coupler between E1 to E2 and E3 to E4. Add a jumper from E2 to E3.

3. If the formatter is equipeed with a 100-pin connector, adapter part No. ACC993A must be used to convert the 100-pin connector to two 50-pin connectors.



H9270 MODULE INSERTION SIDE



DDV11-B Backplane Module Insertion Side

NOTE: Memory can be installed in any slot; it is not priority dependent and does not need to be adjacent to the processor.

Figure 2-1 Typical Backplane Configurations

2.3 Installation

1. Insert the coupler into the selected backplane position. Be sure the coupler is installed with the components facing Row One (1).

   The coupler module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

2. Feed the module-connector end of the formatter I/O ribbon cable set into the computer module area. Install the cable connectors into module connectors J1 and J2. Verify that the connector is firmly seated. NOTE that the ribbon cable connectors are not keyed and therefore can be plugged in backwards. The connectors have a triangle marked on one end to identify pin 1. These triangles on the cable must be lined up with matching arrows on the coupler connectors.

3. Connect the tape-formatter end of the I/O ribbon cables to the formatter I/O connectors. Refer to Table 1-2.

4. Apply power to the computer and verify that the green diagnostic LED indicator on the coupler board is lighted. If the DIAG LEG is not lighted, either power is not applied to the coupler, the coupler board is bad, or the LED is bad.

5. Refer to the tape drive manual for operating instructions and apply power to the tape drive. Install a known good reel of tape on the tape drive and place the tape drive ON LINE.

6. Place the computer in the HALT mode to enable ODT. Using the computer terminal examine location 772 520. The contents of this location should be 000 141. These are the tape drive status bits signifying: ON LINE, BEGINNING OF TAPE, and TAPE READY.

7. Using the computer console device, deposit 60007 into location 772 522. The tape should move forward approximately 6 inches and stop. A file mark should have been written on the tape. Examine location 772 520. The contents of this location should be 040 101 signifying that a file mark has been written and detected.

8. Refer to the DILOG software manual and run the diagnostics.

9. The tape system is now ready for data transfer operations.

SECTION 3

OPERATION

3.0 INTRODUCTION

Prior to operating the system, the tape transport manual covering controls and indicators on the tape drive and procedures for mounting and removing tape reels should be understood. Attention should be given to handling the magnetic tape to prevent loss of data or damage to the tape handling equipment. The following precautions should be observed:

a. Always handle a tape reel by the hub hole; squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oil from fingers attracts dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape; this spreads dirt to clean tape reels and can affect tape drive operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the tape drive or tape storage area. Tobacco smoke and ash are especially damaging to tape and tape drives.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer via the coupler and formatter. When system operation is desired, be sure the tape drive on-line indicator is lit. On-line operation is a function of program commands described in SECTION 4 of this manual.

3.1 Tape Format

For detailed information on tape format characteristics see formatter and tape drive manuals.

3.2 Booting From Magnetic Tapes

1. Place the tape transport "ON LINE" and position the tape at "Beginning of Tape".
2. Load Register location 772522_8 with 10000_8.
3. Load Register location 772524_8 with 177777_8 (-1).
4. Load Register location 772522_8 with 60011_8. The tape will jump forward and halt.
5. Load Register location 772522_8 with 60003_8. The tape will jump forward and halt.
6. Load PSW ($S) with 350_8.
7. Load PC (R7) with 0.
8. Type "P" to start.

3.3 Streaming Tape Transports

With jumper installed on the coupler as described in the Installation SECTION 2.3, the tape transport will function in the lowspeed or STOP/START mode when addressed as logical unit number 0. When addressed as logical unit number 4, the streamer will function in the high speed streaming mode.

SECTION 4

PROGRAMMING

NOTE: For purposes of discussion in this section, whenever the tape "CONTROLLER" or "CONTROL UNIT" is referred to the terms "CONTROLLER" or "CONTROL UNIT" refer to the coupler/tape formatter functional combination.

4.1 Programming Definitions

FUNCTION: The expected activity of the tape system (read, write, rewind).

COMMAND: The instruction which initiates a function (GO, Select).

INSTRUCTION: One or more orders executed in a prescribed sequence that cause a function to be performed.

ADDRESS: The binary code placed on the BDAL0-15 lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip-flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

REGISTER: An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

4.2 Tape Controller Functions and Registers

The tape controller performs eight functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command, and perform a function, the controller must be properly addressed and the tape drives must be powered up, at operational speed, and be ready.

All software interaction between the tape controller, the processor, and processor memory is accomplished by six registers in the tape controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The six controller registers, their addresses, mnemonics, and their bit assignments are shown in Figure 4-1.

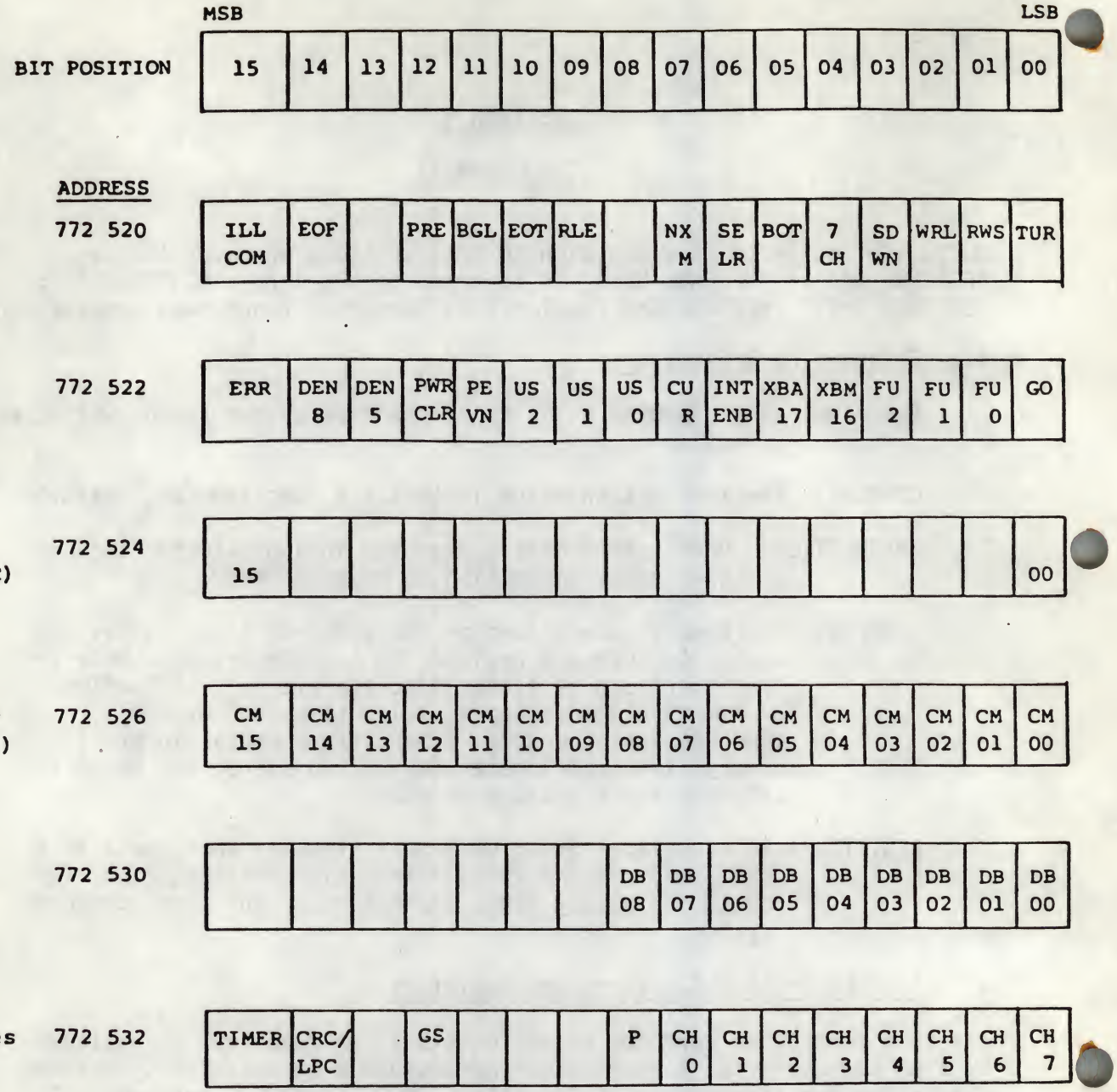


FIGURE 4-1 Coupler Register Configuration

4.2.1 Status Register (MTS)

The address of the MTS register is 772 520. MTS is a read only register. The functions of the bits of this register are as follows:

BIT 15 - ILLEGAL COMMAND: Set by any of the following illegal commands:

1. Any DATO or DATOB to the command register during the tape operation period.

2. A write, write EOF, or write with extended IRG operation when the File Protect bit is a 1.

3. A command to a tape unit whose Select Remote bit is 0.

4. The Select Remote (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO Pulse to the tape unit is not generated. In addition, the CU ready bit remains set.

BIT 14 - END OF FILE (EOF): Set when an EOF character is detected during a read, space forward, or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the File Mark signal upon EOF detection.

BIT 13 - NOT USED

BIT 12 - HARD ERROR (HE): Set as the result of an error being detected on tape.

For all errors, the ERR bit sets at the end of the record. Both lateral and longitudinal parity errors are detected during a read, write, write EOF and write with extended IRG operations. The entire record is checked including the CRC and LOC characters. During a write operation a correctable error in the PE (1600 bpi) mode will set this bit.

BIT 11 - BUS GRANT LATE (BGL): Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the controller receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

BIT 10 - END OF TAPE (EOT): Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

BIT 9 - RECORD LENGTH ERROR (RLE): Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.

BIT 8 - BAD TAPE ERROR (BTE): NOT USED

BIT 7 - NON-EXISTENT MEMORY (NXM): Set during NPR operations when the control unit is bus master, and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

BIT 6 - SELECT REMOTE (SELR): Cleared when the tape unit addressed does not exist, is offline, or has its power turned off.

BIT 5 - BEGINNING OF TAPE (BOT): Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

BIT 4 - SEVEN CHANNEL (7CH): Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.

BIT 3 - TAPE SETTLE DOWN (SDWN): Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

BIT 2 - WRITE LOCK (WRL): Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.

BIT 1 - REWIND STATUS (RWS): Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction)

BIT 0 - TAPE UNIT READY (TUR): Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

4.2.2 Command Register (MTC)

The address of MTC is 772 522. The functions of the bits of this register are as follows:

BIT 15 - ERROR (ERR): Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.

BITS 14-13 - DENSITY (DEN 8, DEN 5): NOT USED. Not applicable on 9 track tape.

BIT 12 - POWER CLEAR (PCLR): Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.

BIT 11 - LATERAL PARITY (PEVN): Not applicable for 9 track tape.

BIT 10 - UNIT SELECT 2: Specifies one of two possible formatters. Selects the high-speed streaming mode on streamer type tape transport.

BITS 9-8 - UNIT SELECT 1: Specifies one of the four possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

BIT 7 - CU READY (CUR): Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal, all commands it receives while the CU Ready bit is 1.

BIT 6 - INTERRUPT ENABLE (INT ENB): When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit i.e., CU READY or ERROR = 1.

BITS 5-4 - ADDRESS BITS: Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

BITS 3-1 - FUNCTION BITS: Selects 1 of 8 functions (programmable commands).

BIT 3	BIT 2	BIT 1	
0	0	0	Off line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write with Extended Interrecord Gap
1	1	1	Rewind

BIT 0 - GO: When set, begins the operation defined by the function bits.

4.2.3 Byte Record Counter (MTBRC) (The address of MTBRC is 722 524)

The MTBRC is a 15-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward of space reverse operation. When used in a write or write with extended IRG Operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unti will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of bytes to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 3's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

4.2.4 Current Memory Address Register (MTCMA) (The address of MTCMA is 772 526).

The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 2 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 2 of the last characters in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

4.2.5 Data Buffer (MTD) (The address of MTD is 772 530).

The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In a DMA operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 8 respectively. Bits 0 through 7 are set or cleared on a processor DATA. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

4.2.6 Tape Read Lines (MTRD) (The address of MTRD is 772 532)

The memory locations allocated for the tape read lines are:

Bits 0-7 for the channels 7-0 respectively.
Bit 8 for the parity bit.
Bit 12 for the gap shutdown bit.
Bit 13 not used.
Bit 14 for the CRC, LPC character selector.
Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) are at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATO except that bit 13 reads back as a 0.

4.2.7 Timer

TIMER is a a 10 kHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SECTION 5

TECHNICAL DESCRIPTION

5.0 INTRODUCTION

This section contains the theory of operation of the DQ130 tape coupler. The text references block and timing diagrams interspersed with text, a Glossary of Terms in Appendix B, and detailed logic diagrams in SECTION 6. The material begins with a General Description followed by a Functional Description.

The General Description describes the interconnection of the major logic elements that make up the coupler. The principle reference is the simplified block diagram. The Functional Description describes the individual logic elements within the coupler. The text is referenced to the detailed block diagram. The description assumes an understanding of the LSI-11 I/O bus and a basic understanding of digital computer theory.

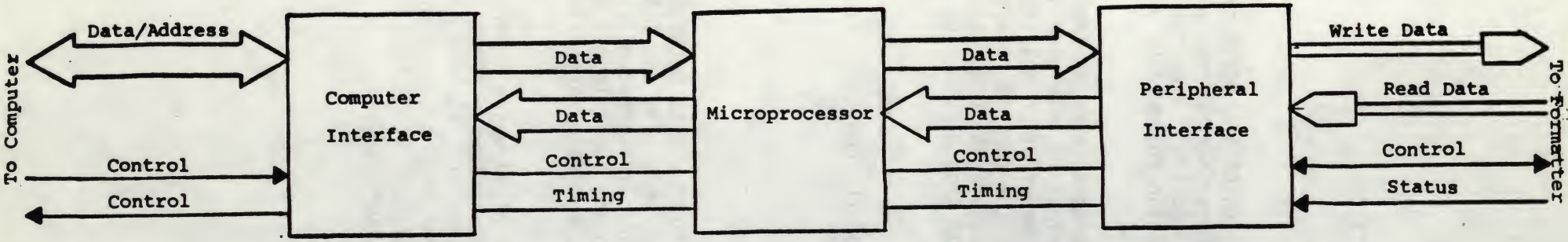
5.1 General Description

Figure 5-1 is a simplified block diagram of the coupler. The coupler comprises three logical sections:

a. Computer interface
b. Microprocessor
c. Formatter interface

The three sections function together to transfer data between the I/O bus of the computer and up to eight tape drives. The two interface sections match the voltage levels and load/drive characteristics of the computer I/O bus and tape I/O lines to the logic levels of the coupler. The microprocessor is the control, timing, and data conversion section of the coupler.

The microprocessor functions under control of firmware instructions stored in solid state, programmable, Read Only Memory (PROM). The microprocessor is implemented with AM2900-series bit-slice microprocessor chips. Refer to "MICROPROGRAMMING HANDBOOK" from Advanced Micro Devices, Inc., 1901 Thompson Place, Sunnyvale, California 94086 for introductory material on microprogramming a bipolar microprocessor.



- Buffer I/O Lines
- Bus Sequence
- Address Decode

- Timing Source
- Control Center
- Error Checking
- Register Storage
- Data Buffering

- Buffer I/O Lines
- Set Disc Configuration
- Parallel-To-Serial And Serial-To-Parallel Data Conversion
- Clock Synchronization

FIGURE 5-1: Simplified Block Diagram
Tape Coupler

5.1.1 Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q bus of the computer and the coupler and (2) synchronize information transfers. There are two major classes of lines connected to the computer interface:

a. Data/address lines
b. Control lines

There are 15 bidirectional data/address lines. Both device addresses and data are transferred over these lines. Address information is first placed on the lines by a bus master. The bus master then either receives input data from, or outputs data to, the addressed slave device, or memory, over the same lines. During initialization and status-transfer sequences, the coupler is a slave and is selected by address 224_8. During data transfers, the coupler is bus master and either receives data from, or outputs data to, the processor memory via the DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and originate either at the processor or at the coupler.

The computer interface controls the synchronization, or "bus arbitration" sequence. Bus synchronization is done by a separate hardware state processor, rather than by the microprocessor, to minize bus use by the coupler. This permits other devices to use the DMA channel on a time multiplexed basis with the tape coupler.

5.1.2 Microprocessor

The microprocessor is the timing and control center of the coupler. The microprocessor is controlled by instructions stored in programmable read only memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the computer. The instruction operands are stored in registers within the microprocessor.

When a GO command is issued by the computer, the firmware microinstructions cause the registers to be examined, and either a data transfer sequence or a rewind sequence to be performed - not that rewind functions can be performed on any tape drive not involved in a data transfer operation simultaneous with data transfers.

The microprocessor contains an eight word RAM memory dedicated to buffering data between the Q bus and the microprocessor. This allows several DMA cycle requests to be missed without missing data words being transferred between the tape and computer memory.

The rate and order (format) at which data is transferred to the tape is controlled by the microprocessor. Within the microprocessor, data is handled in 8-bit parallel bytes. Error check bits are calculated (LRCC, CRCC) and supplied to the tape during a write function. During a read function, the microprocessor monitors the error check bits and the data being read. Discrepancies are flagged as errors to the computer. The microprocessor detects other types of errors during the transfer functions (data late, programming error, etc.) and monitors status lines from the tape for malfunctions within this assembly. All errors are assembled into a status word for access by the processor.

5.1.3 Peripheral Interface

The purpose of the peripheral interface is to match the characteristics of the tape formatter to the characteristics of the microprocessor. The peripheral interface:

a. Contains line drivers and receivers that buffer the information lines between the coupler and the tape drives over cable lengths up to 20 feet.

b. Contains the PROM and jumpers that permit configuring the coupler to match the different tape subsystem configurations.

5.2 Functional Description

The detailed block diagram (Figure 5-2) shows the functional elements of the tape coupler. A circled number, within the blocks of the diagram references the sheet of the detailed logic drawing represented by the block. The detailed logic drawings are in SECTION 6. A Glossary of Terms, in Appendix B, defines mnemonics used in this text and on the logic drawings.

5.2.1 Computer Interface

The Computer interface comprises the following elements:

a. Data/Address Receivers.
b. Control Receiver/Drivers
c. Data/Address Drivers
d. Bus and Arbitration Sequence (Hard-wired state processor)

The computer interface is a hard-wired logic section that buffers and synchronizes information transfers between the I/O bus and the coupler.

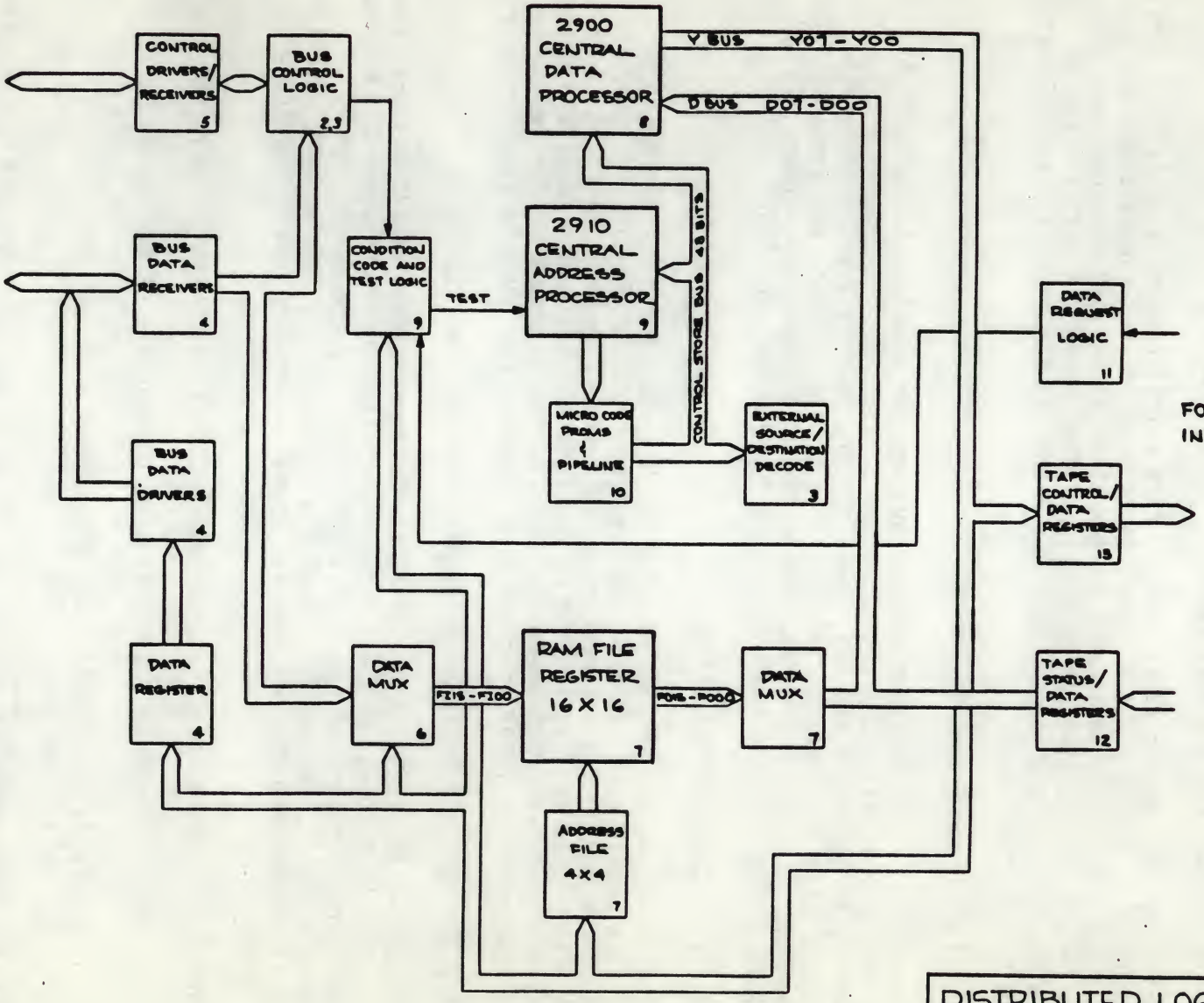


FIGURE 5-2 DQ130 BLOCK DIAGRAM

DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM DQ130		SHT 1 OF 13
		DRAWING NUMBER 853016

5.2.1.1 Data/Address Receivers

Both data and device addresses are time multiplexed on a 16 I/O bus line ($BDAL00_L$ - $BDAL15_L$). The tri-state receiver/driver circuits H0, H8, H10, and H11 shown on sheet 4, buffer these lines into the coupler. Once buffered, the received lines are identified as DB00 - DB15 and routed to the bus arbitration sequence logic and the RAM data file multiplexer in the microprocessor.

5.2.1.2 Control Receiver/Drivers

The control lines between the I/O bus and the coupler are buffered by circuits F11, F12, H12, and H13 shown on sheet 5. The receivers are always connected to the bus. Setting circuit pins 7 and 9 low enables the tri-state drivers to the bus. Two of the circuits are permanently enabled; circuit H12 is enabled by Transmit Select Achnowledge (TSACK), and circuit H13 is enabled by Device Enable ($\overline{DEN}$) and $\overline{TSACK}$.

5.2.1.3 Data/Address Drivers

The tri-state drivers in circuits H8, H9, H10, and H11 are enabled by Device Enable ($\overline{DEN}$) to gate addresses and data to the I/O bus. Addresses and data to the I/O bus are temporarily stored by register circuits E9 and F9. Information from the FQ bus is clocked into the registers either by a signal Data (DA) or by signal Load Address (LDADD). The least significant bit (D00) is gated with control term TD00G to the line drivers.

5.2.1.4 Bus and Arbitration Sequence (State Processor)

To ensure fastest response time, the synchronization of I/O bus transfers is done by hard-wired state logic illustrated on sheets 2 and 3. Information transfers are of two kinds; programmed I/O and direct memory access (DMA). During DMA transfers, the coupler is bus master. Distinguishing between the two transfer types is the function of the arbitration logic.

The bus sequence logic synchronizes master/slave transfers over the I/O bus.

Transfers between the I/O bus and the coupler are of two types:

a. Register transfers via programmed I/O.
b. Data transfers via DMA.

During programmed I/O transfers, the seven coupler registers are accessed; initialization information is transferred to the registers; status information is accessed from the registers. The registers are located in the μ data file. Address information from the processor is decoded by circuits D4 and D5. Circuit D5 decodes the 7774 portion of the address word; circuit condition of the four least significant bits which are buffered to become A00 - A03. Figure 5-2 shows the registers selected by specific configurations of these bits. Note that bits A00 - A03 are used throughout the bus and arbitration sequence logic.

The bus and sequence arbitration logic primarily comprises PROM's, used as decoders, and flip-flops that temporarily store control information. For example, the storage elements for the DMA light, the Busy light, and the Diagnostic light are contained in this logic. Monostable multivibrators F2-5 and F1-13 monitor bus activity to insure responses to the bus master occur within 10 microseconds. Circuits Y1 and E1 establish the crystal-controlled time base for the coupler. The 10 megaHertz output of E1 is divided by two to generate 200 nanosecond clock PCLK buffered to become PPCLK, $\overline{\text{PPCLK}}$, and $\overline{\text{CLK}}$*.

5.2.1.5 Bus Transfer Timing

The two major types of transfers are divided into the following I/O operations and an interrupt sequence:

- Data Input Transfer (DAT1) slave
- Data Output Transfer (DATO) slave
- Data Input Transfer (DAT1) DMA
- Data Output Transfer (DATO) DMA
- Interrupt Requests

Programmed I/O transfers are initiated with the coupler when the computer places the device address of the coupler on the BDAL04 through BDAL15 lines, sets the BBS7L signal at a low level, and switches signal BSYNCL low. Within the coupler, BSYNCL converts to RSYNC.

Address decoder D5 monitors the address lines. When the coupler address is decoded and RSYNC is asserted, the Bus Active (BACTFF) sets. This sets in motion the transfer sequence.

The sequence for a DATI operation is shown in Figure 5-3. For a DATI sequence, the state processor steps through states 1, 2, and 7. The coupler responds to input requests by asserting TRPLY within 10 microseconds of a DATI request. DATI operations read status from the coupler.

The sequence for a DATO operation is shown in Figure 5-4. DATO operations transfer commands to the coupler registers. A DATO is similar to a DATI. The principle difference is that during a DATO, the Data Out FF rather than the Data In FF is set and the Data Available (DA) signal is not generated.

DMA transfers are between the coupler and computer memory. The coupler is always bus master. There are two transfer types: data in to memory (DATI) and data out of memory (DATO). Once the coupler has been granted DMA bus control, the transfer sequence is similar to I/O bus transfers.

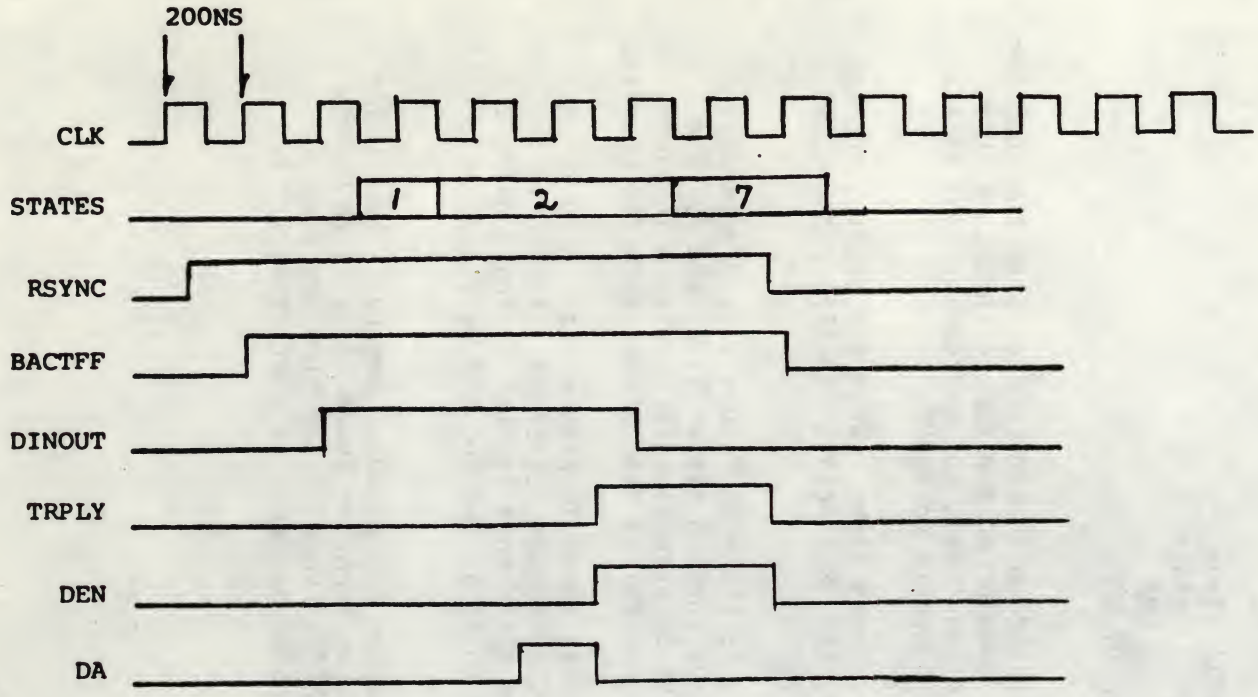


Figure 5-3: DATI - SLAVE, Q BUS

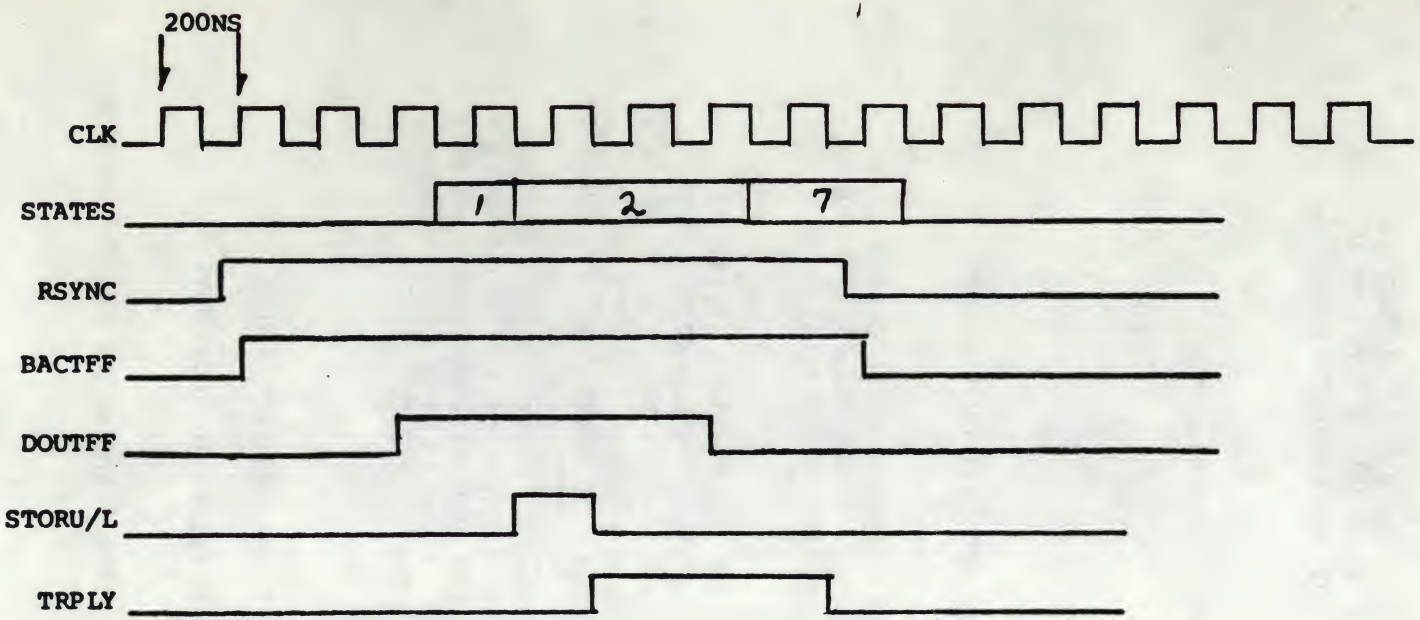


Figure 5-4: DATO - SLAVE, Q BUS TRANSFERS

Figure 5-5 illustrates the DMA DATI timing; Figure 5-6 illustrates the DMA DATO timing.

Interrupt request timing is illustrated by Figure 5-7. Interrupt requests are originated by Memory Request A (MRQA), a function of YOO bit and the FUNC signal. The interrupt vector address is 224_8.

5.2.2 Microprocessor

The microprocessor comprises the following major elements:

a. μ Data File
b. μ Data File Address Register
c. μ Data File multiplexer
d. 2901A Array and Status Register
e. Control Memory and Register
f. Control Store Address Programmer and Test Multiplexer
g. D Bus Multiplexer

The preceding elements are interconnected to perform the control, timing, error checking, and data manipulation functions of the coupler. Information is transferred among the elements over internal buses defined by Table 5-1.

A microprocessor functions under control of instructions stored in read only memory (ROM or PROM). These instructions are called micro-instructions because most often a series of them is required to perform a function. All of the microinstructions are called firmware since, once stored in PROM, they cannot be altered. To understand the function of a microprocessor, please refer to "The Microprogramming Handbook" from Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, California 94086. Detailed technical descriptions of the 2901A four-bit bipolar microprocessor slice and of the 2901 microprogram coupler are given in the Advanced Micro Devices "AM2900 Family Data Book". These two elements are the major components of the coupler.

5.2.2.1 Micro Data File

This 16 word, 16-bit each word, data file has two functions:

a. Storage for the seven coupler registers in locations 9_{16} through F_{16} as follows:

b. Buffer storage for data words being transferred via DMA between memory and disc (locations 0 through 7).

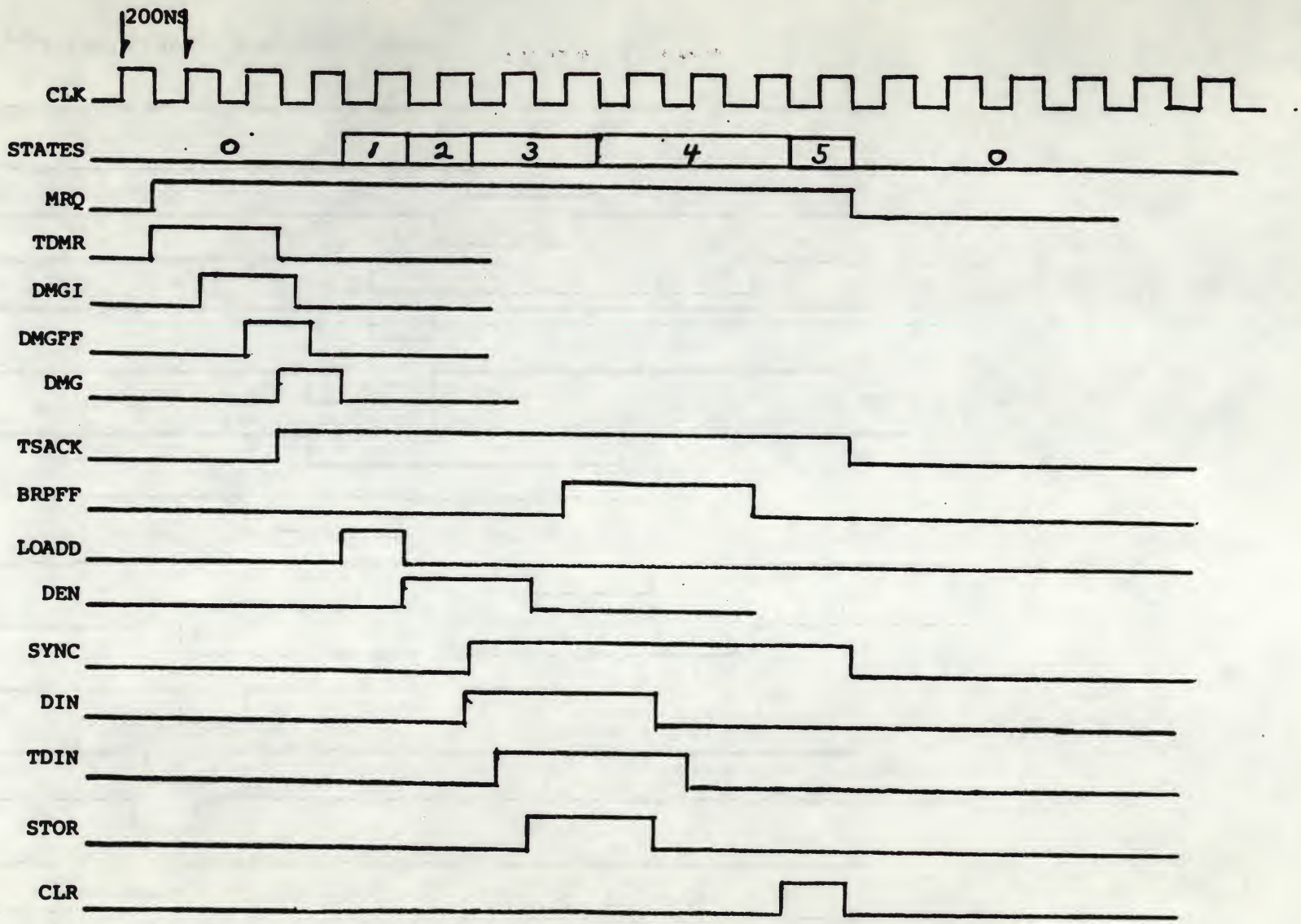


Figure 5-5: DATI - Q BUS DMA TRANSFERS

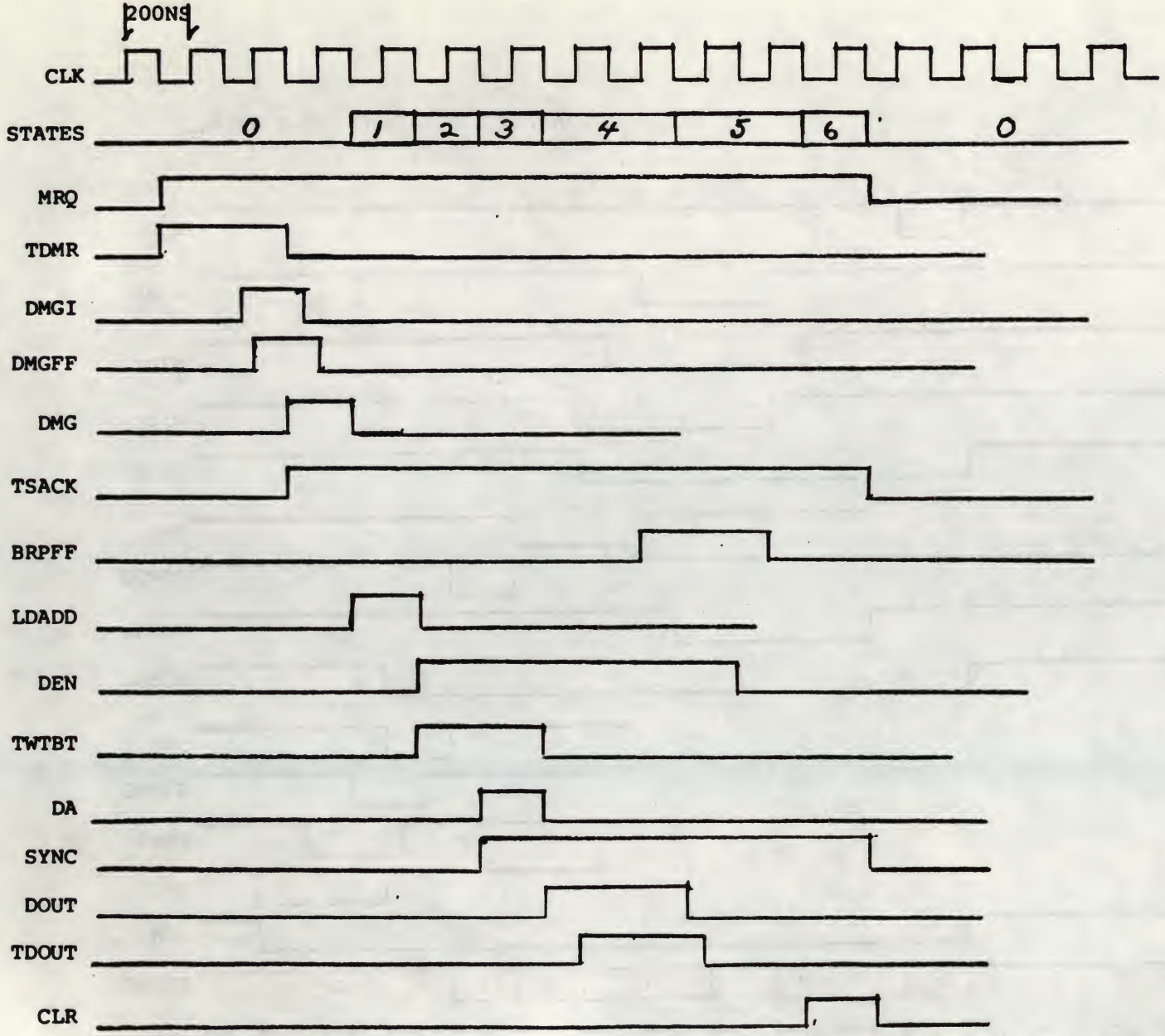


Figure 5-6: DATO - Q BUS DMA TIMING

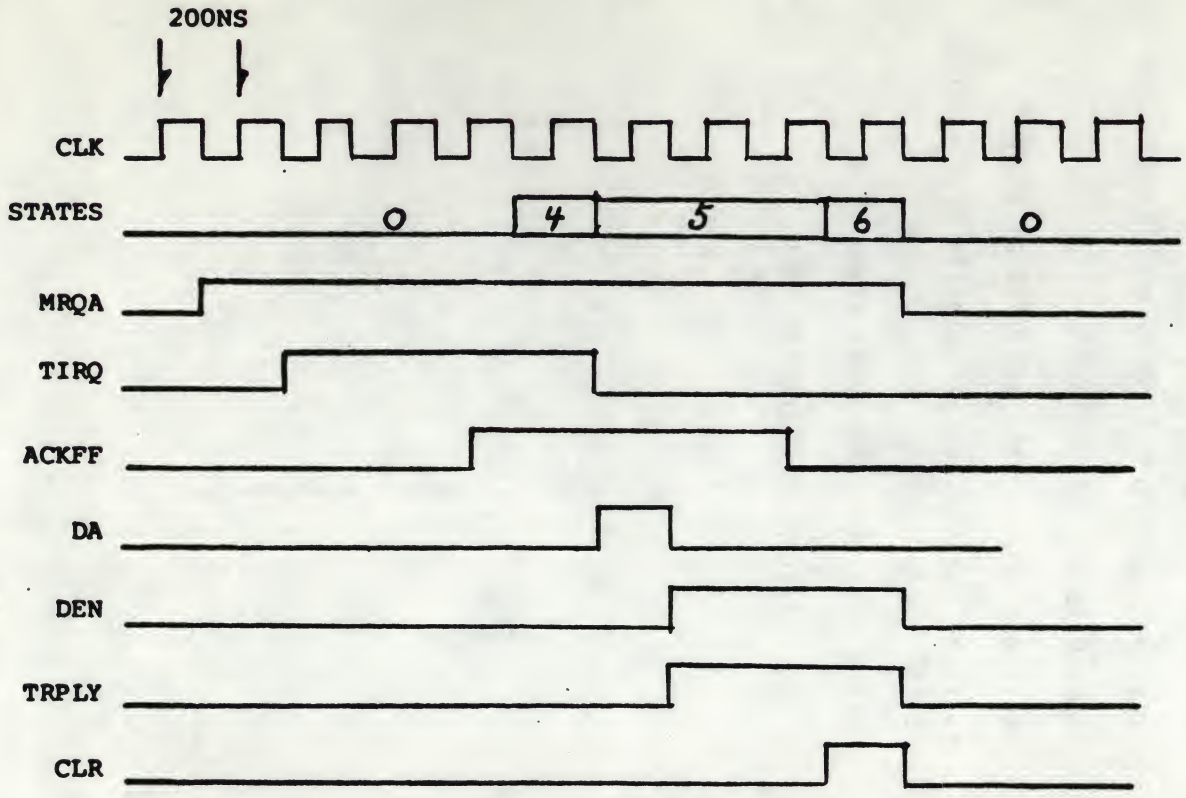


FIGURE 5-7: INTERRUPT SEQUENCE TIMING

TABLE 5-1: COUPLER BUSES

The following prefixes are used as bus identifiers in the following discussion and in the schematic diagrams in SECTION 6.

DESIGNATION	FUNCTION
B	LSI-11 I/O bus: Data, Address and Control lines bidirectional.
DB	Data bus FROM I/O bus receivers into coupler.
D	Input Data bus to 2901A.
P	Peripheral Bus: Data and Control signals.
T	Transmit data or control signals from coupler to LSI-11 I/O bus.
Y	Output data bus from 2901A array.
FQ	Output of 16 x 16 Microdata file.

TABLE 5-2: COUPLER REGISTER STORAGE

REGISTER	FILE LOCATION (HEX)
RKDB	9
RKDA	A
RKBA	B
RKWC	C
RKCS	D
RKER	E
RKDS	F

Sheet 7 shows the data file. Inputs to the data file are from the data file multiplexer on lines FI00 - FI15. Outputs from the data file are on lines FØØØ - FO15 to the microdata bus. Data file locations are accessed by the address file and by the DS2 portion of the control register word. Note that the data file is separated into 8-bit bytes and that the upper byte (FX08 - FX15), the lower byte (FX00 - FX07), or both bytes can be written into or read from.

5.2.2.2 Micro Data File Addressing

The microdata file address logic is shown on Sheet 7. Two sources address the data file:

a. The bus and arbitration sequence logic (circuit E5).
b. The 4 x 4 address file (circuit F5)

address control from the bus and arbitration sequence logic is address lines A01 - A03, which select specific coupler registers.

The 4 x 4 address file is capable of storing up to four addresses. The source of address information to the address file is bit 03 of field three of the control register word (CR3-03) and bits 00, 01, and 03 of the Y bus. Information can be read from and written into different locations of the address file simultaneously. When addresses are being buffered through circuit E5, circuit F5 is disabled from supplying addresses. Write and read addresses to the address file are from field three of the control register word directly, and indirectly via PROM AB14 (Sheet 8).

5.2.2.3 Micro Data File Multiplexer

The microdata file multiplexer, shown on Sheet 6, switches the input to the microdata file between two sources; the contents of the Y bus, and the contents of the data bus (DB). The contents of field three of the control register word control the selection. Note that bits 8 and 15 to the multiplexer from the data bus can be selected by circuits E10 and E11 to be either DB8 and 15 or file output bits 8 and 15 restored in the file.

5.2.2.4 2901A Array and Status Register

The 2901A array is shown on Sheet 8. The status register is shown on Sheet 9 (circuit DE14). The 2901A array comprises two AM2901A four-bit bipolar microprocessor slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. The major sections of the AM2901 are shown within dashed lines on the block diagram. A description of the operation of this device is given in the "AM2900 Family Data Book".

The D bus supplies external data to the 2901A data from the 2901A is on the Y bus. Control inputs to the 2901A are as follows:

TABLE 5-3: CONTROL INPUTS TO 2901A

MNEMONIC	SIGNAL SOURCE	DEFINITION
A0-3	Control Register	Address inputs; selects the A file register contents to be connected to the 2901A, A bus. (S1)
B0-3	Control Register	Address inputs; selects the A file register contents to be connected to the 2901A, B bus. (S2)
I0-8	Control Register	Instruction control lines; lines 0-2 select the data sources to be applied to the ALU; lines 6-8 determine the routing of the output of the ALU within the ALU and the source of data supplied to the Y (output) bus.
CN	Control Register	Carry input of ALU. Used during arithmetic operations.
CP	Crystal Oscillator	200 nanosecond clock to 2901A.

The status register is updated on a coupler clock with the ALU status. The register stores the following conditions:

TABLE 5-4: STATUS REGISTER BITS

MNEMONIC	DEFINITION
C_s	Indicates a "carry out" of ALU
N_s	The most significant ALU bit (sign of result).
V_s	Overflow has occurred.

5.2.2.5 Control Memory and Register

The control memory stores the firmware that controls the operation of the coupler. It comprises six 512 x 8 bit programmable read-only-memories (PROMs) identified as D9, D10, D11, D12, F13, and F14, on Sheet 10. The Proms have a pipeline register at the output identified as the Control Register (CR). The six PROMs produce a 48-bit instruction word divided into six 8-bit fields. Figure 5-8 depicts the instruction word.

The contents of the control memory are accessed by the Control Store Address Processor and strobed into the control register by the PPCLK clock. The contents of the control register (CR1-00-07 through CR5-00--7 and literal D00-D07) are routed throughout the logic of the coupler.

5.2.2.6 Control Store Address Programmer

The control Store Address Programmer (CSAP) is an AM2910 microprogram control circuit and is described in the "AM2900 Family Data Book". It controls the sequence of execution of microinstructions stored in the control memory. The CSAP is shown on Sheet 9.

Control Store output address lines CSA00 through CSA08 select one of 512 locations in control memory and are also routed to test connector J2. Inputs to the CSAP are primarily from fields four and five of the control register and the $\overline{\text{TEST}}$ output of test conditions multiplexer C13 (shown on Sheet 9). Bits 00 through 07 (LSB) of field five (CR5) supply branch addresses to the CSAP. Bits 00 through 03 of field four (CR4) supply instruction codes to the CSAP. Any one of 16 instructions can be selected. The instructions can be modified by the state of the $\overline{\text{TEST}}$ input. The instructions select the next source of addresses to the control memory. The primary sources of addresses are as follows:

a. A program counter/register within the CSAP.
b. A five word stack within the CSAP.
c. Branch addresses directly from bits 00-07 of field five (CR-5).

Note that bits 04 through 06 of field four (CR4) control test condition multiplexer C13. This multiplexer connects one of seven selected conditions to the $\overline{\text{TEST}}$ line when specified by the current microinstruction being executed. The conditions tested for are shown on the following Table 5-5:

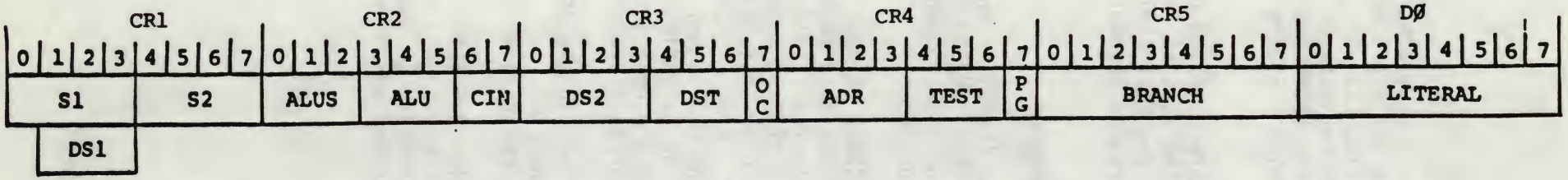


FIGURE 5-8 Microinstruction Word

TABLE 5-5: ADDRESS MODIFICATION CONDITIONS

MNEMONIC	CONDITION
C	No carry from 2901A ALU.
Z	ALU result is zero.
C	Carry from ALU.
N	ALU sign bit is logical true.
V	ALU has overflowed.
INIT	Initiate

Note that bus signal BDCOKH if ever low disables the output of the CSAP and generates a Reset (RST) signal.

5.2.2.7 D Bus Multiplexer

The D bus multiplexer, shown on Sheets 7, 9, and 12, is the information source to the 2901A array processor. The multiplexer comprises circuits D8 (Sheet 9), E8 and F8 (Sheet 7), and B9(Sheet 12). Circuits B7, B8, and B9 also function as storage registers. One additional information source for the D bus is PROM D9, shown on Sheet 10, which supplies the literal (LIT).

Field one CR100-03 and CR2-00 via circuit E12 (Sheet 3) gate the selected source to the D bus. Information sources to the D bus are as follows:

TABLE 5-6: INFORMATION SOURCES TO D BUS

CIRCUIT	SHEET	SOURCE
D9	10	Literal from control memory
E8, F8	7	RAM File data bus upper and lower bytes
D8	9	Coupler status
B7	12	Data from tape
B8, B9	12	Tape status

5.2.3 Peripheral Interface

The peripheral interface comprises the following elements:

a. Peripheral input output registers
b. Data request logic
c. Cable driver/receivers and control buffers

5.2.3.1 Peripheral Input Output Registers

There are two registers which temporarily store information being transferred between the tape and the other elements of the coupler; an input register and an output register. The input register is shown on sheet 12, and the output register on sheet 13.

The input register stores status information and data received from the tape and comprises circuits B7, B8, and B9. The outputs of these circuits are gated to the D bus as described in paragraph 5.2.2.7. The tape status information originates at line receivers and is stored in circuit B9; the data from the tape is stored in circuit B7.

The output register stores information to be sent to the tape and comprises circuits A8, A9, and A10 on Sheet 13. These circuits make up a 32-bit register that receives information from the Y bus in 8-bit segments. Y bus information is stored in the register under control of the PIA, PIB and PIC clocks. The outputs of the register are routed to the tape formatter.

SECTION 6

TROUBLESHOOTING GUIDE

6.0 INTRODUCTION

The purpose of this section is to assist the maintenance engineer in isolating malfunctions to specific assemblies of the tape based computer system. Normally, once a malfunctioning assembly (tape drive, memory, coupler, CPU board, etc.) is located, a known good assembly should be substituted while the malfunctioning unit is returned to a repair depot. Be sure to read carefully paragraph 6.2, Operating Precautions, before troubleshooting the system.

6.1 General

System malfunctions come under two major classifications; intermittent and continuous. Intermittent failures are normally very difficult to isolate and usually require step-by-step substitution of equipment over a period of time until the intermittent assembly is isolated. This section will primarily discuss continuous failure isolation.

When troubleshooting electronic equipment, certain basic items should always be checked:

a. Is power properly applied to all system assemblies - switches on, fuses good, AC power cords plugged in, area power circuit breakers on, etc.

b. Check DC power at backplane terminals of computer - +5V DC, +12V DC. If DC voltages are low, verify AC line voltage is within tolerance:

   100 - 127 Vrms, 50±1Hz or 60±1 Hz

   200 - 254 Vrms, 50±1Hz or 60±1Hz

c. Verify system generates proper response when system is powered-up (refer to operation instructions for the processor).

d. Verify all modules are properly plugged in. No empty slots should exist between modules.

e. Verify all signal cables (tape, console terminal) are properly plugged in. Check each end of cables.

f. Can the console be operated in "Local" mode? If not, console is defective.

g. Is the tape drive READY light on?

h. Are the computer panel switches set correctly (ENA/HALT, LTC, etc.)?

i. Is green DIAG light on tape coupler board on?

6.2 Operating Precautions

While troubleshooting the system, the engineer should check the following items:

a. Is the tape clean? Dirty tape or tape read/write heads cause bit dropouts.

b. If tape produces a high-pitched whine or metal-to-metal sound, immediately power down the tape; a bad bearing is possible.

c. Was any module pulled out or plugged in while power was applied? Shorting connector pins together can cause an integrated circuit to fail.

d. Has ribbon cable connector been plugged in upside down at coupler? This connector is not keyed. Be sure the arrows on the female connector line up with arrows on male connector.

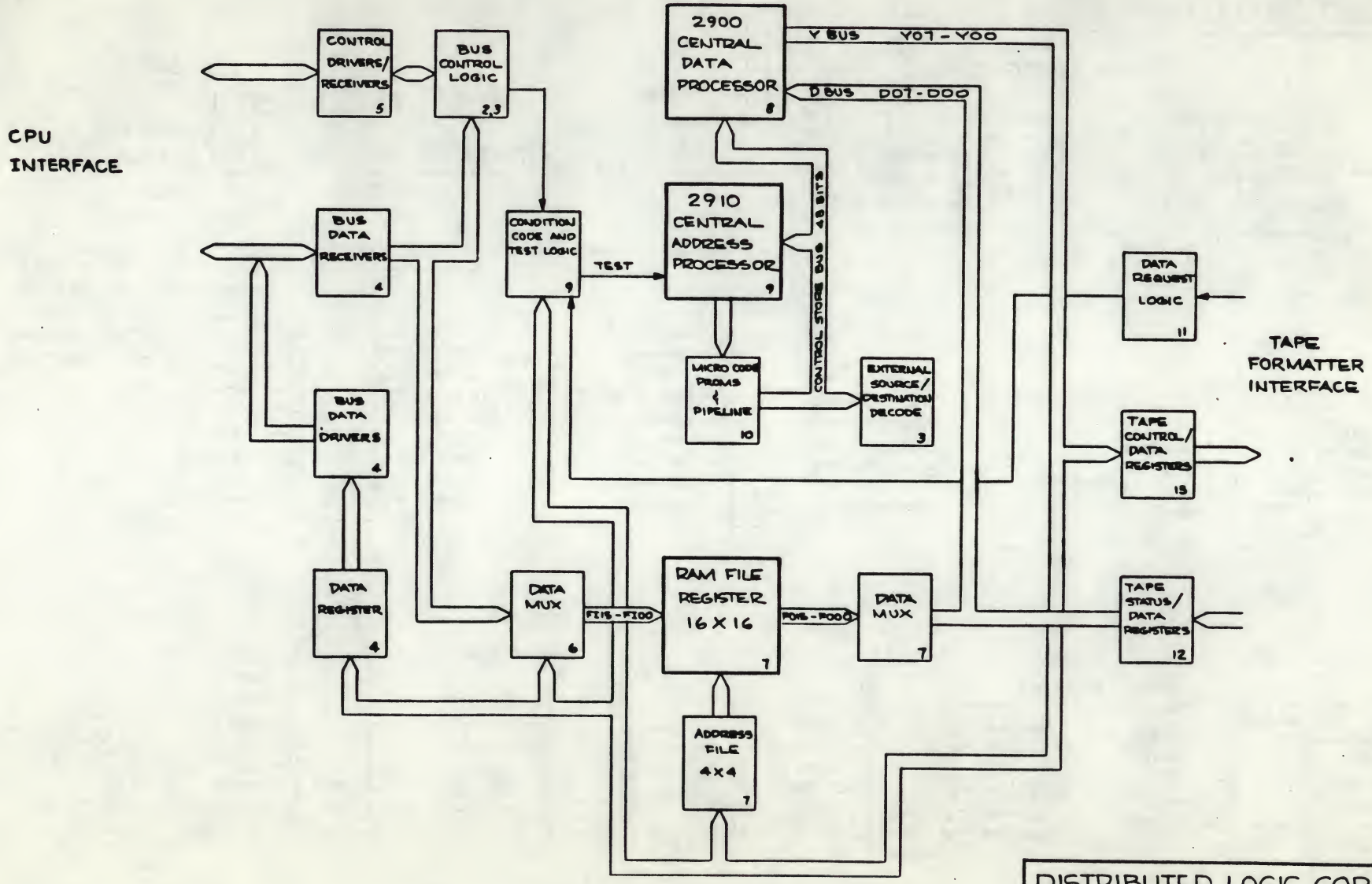
6.3 Possible Troubles

This paragraph provides possible malfunction locations based on either visual indications or tests and assumes the basic items in paragraph 6.1 have been checked and found normal.

NOTE: Before troubleshooting the system, be sure proper operating procedures are being followed and the system is properly configured. Refer to SECTIONs 2 and 3 of this manual or the USER'S GUIDE

The following pages contain a trouble chart. Space is left on the chart for field failures not in the chart to be noted.

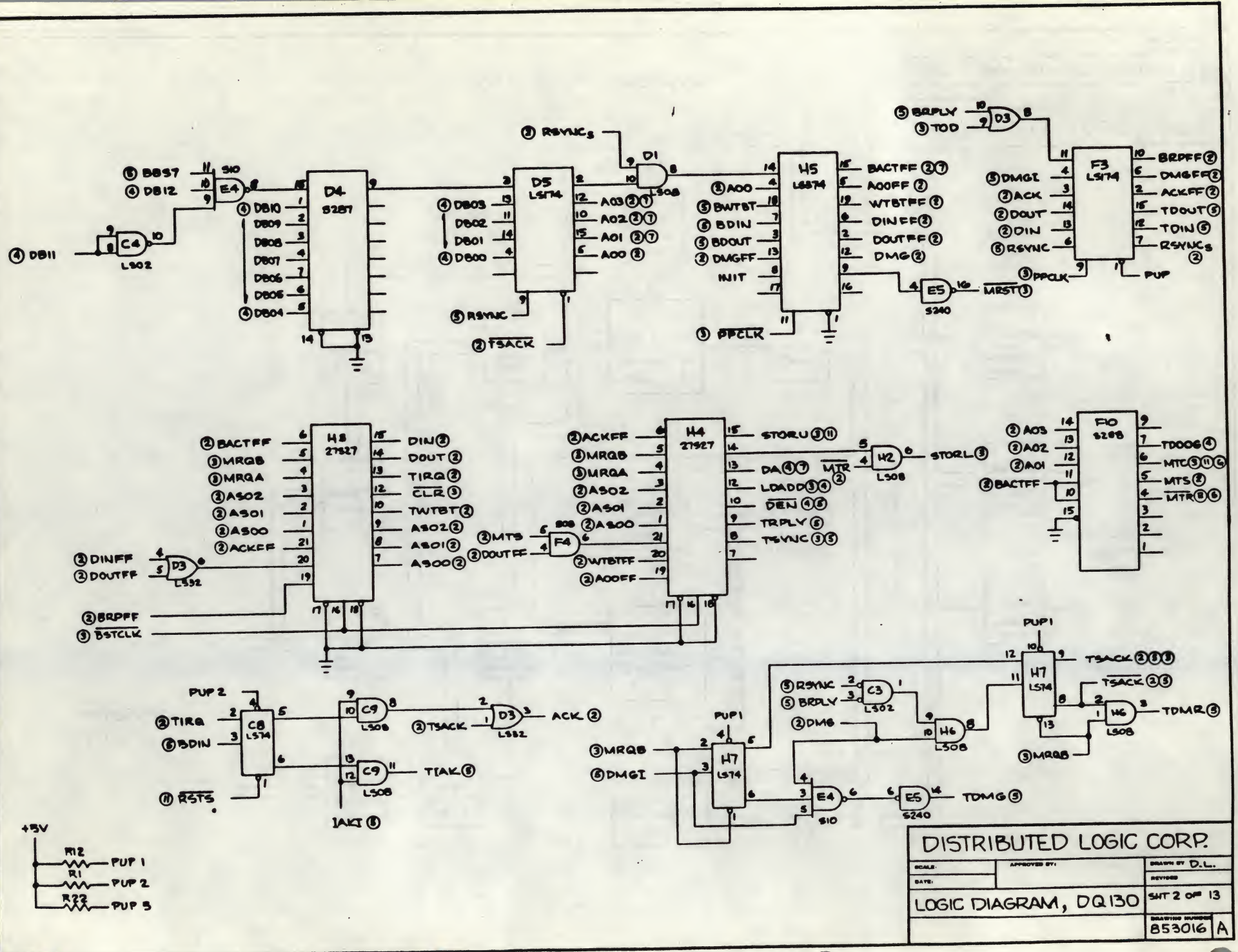
TROUBLE	POSSIBLE CAUSE	CHECK/REPLACE
1. GREEN DIAGnostic light on coupler is OFF.	1. Microprocessor section of coupler inoperative.	1. Coupler.
	a. Crystal not seated in socket or in wrong.	Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or "stuck low", or half-amplitude pulses. If no switching, either power or crystal bad.
	b. Short or open on board.	
	c. Bad integrated circuit.	
	d. No DC power.	
2. No communication between console and computer.	2. I/O section of coupler "handing up" QBus.	2. Computer interface logic of coupler.
	a. $\overline{\text{DEN}}$ always low.	a. Check signal DEN for constant assertion.
	b. Shorted bus transceiver IC.	b. Check I/O IC's. Remove coupler board to see if trouble goes away.
	c. Bad CPU board	c. Run CPU diagnostics.
3. No data transfers to/from tape. BSY light never lights.	3. Tape not ready or bad cable connection.	3. Check tape switches and cable connector.
	a. Improper communication with tape registers on coupler or bad IC in register section of coupler.	a. Load and read tape registers from console with processor halted, i.e., RKDS, RKDA, RKER. Verify bits loaded can be read.
4. Data transferred to/from tape inccorrect. DMA and BSY lights blink to indicate transfers.	4. Bad memory board in backplane.	4. Run memory diagnostic.
	a. Noise or intermittent source of DC power in computer.	a. Check AC and DC power.
	b. Bad IC in tape I/O section of coupler.	b. While operating, check lines from coupler to tape with a 'scope for short or open.
	c. Run tape diagnostic, set console to make system "Halt On Error."	c. Analyze error halt.
	d. Bad area on tape.	d. Errors should always occur in same sector of tape.
	e. Head worn.	e. Replace head.
	f. Crystal in coupler wrong frequency.	f. Check characteristics of tape drive.
	g. Configuration switch J4 not set properly.	g. Check configuration paragraph of Installation Section.



DQ130 BLOCK DIAGRAM

DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		DEVISED
LOGIC DIAGRAM DQ130		SHT 1 OF 13
		DRAWING NUMBER 853016


D4 8287
D5 LS174
H5 LS374
F3 LS174
H8 27S27
H4 27S27
F10 S288
H7 LS174
H6 LS08
C8 LS74
C9 LS08
D3 LS32
F4 S08
H2 LS08
E4 S10
E5 S240
C4 LS02
C3 LS02
D1 LS08
+5V
R12
R1
R22
PUP 1
PUP 2
PUP 3
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LOGIC DIAGRAM, DQ130
SHT 2 OF 13
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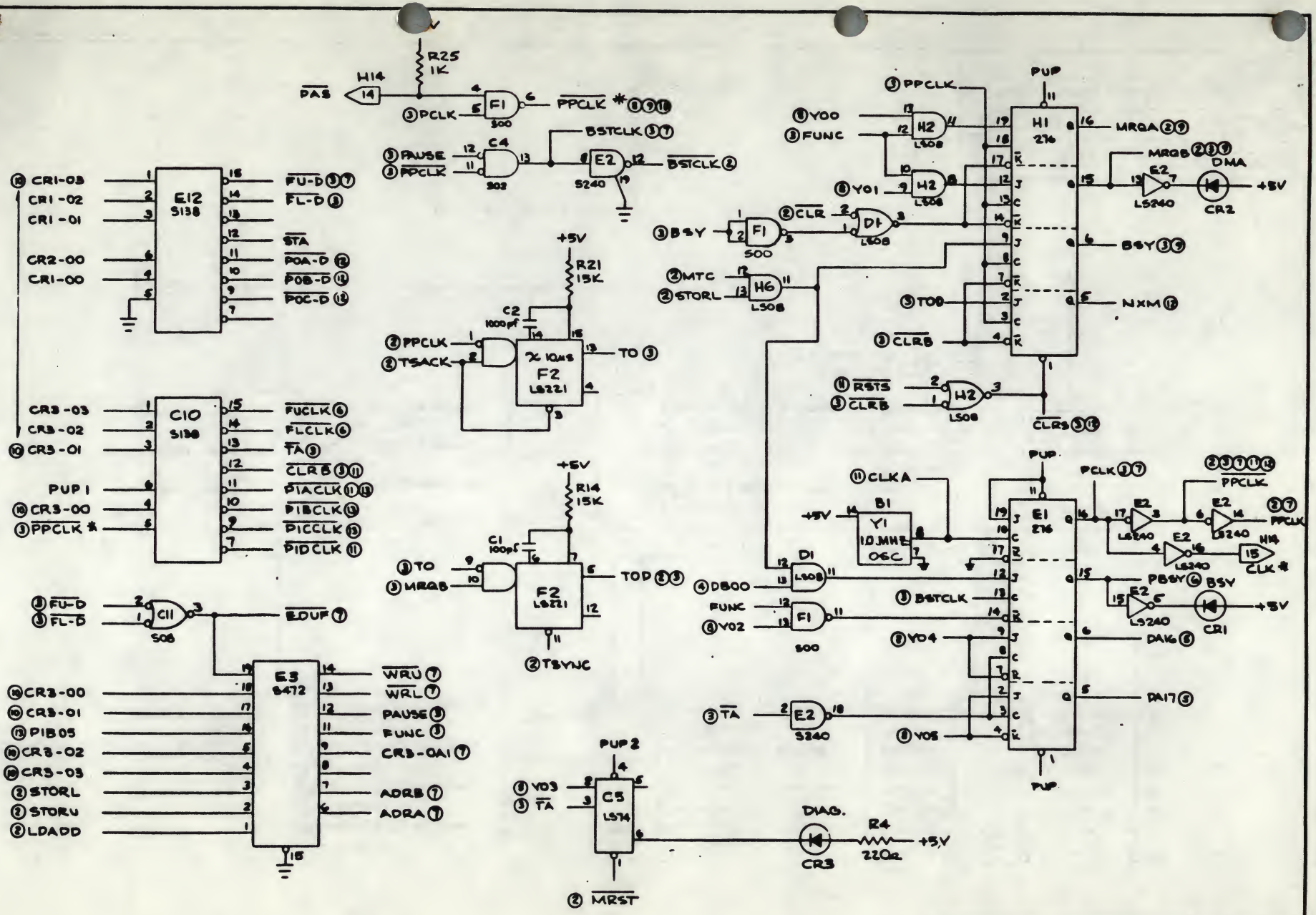
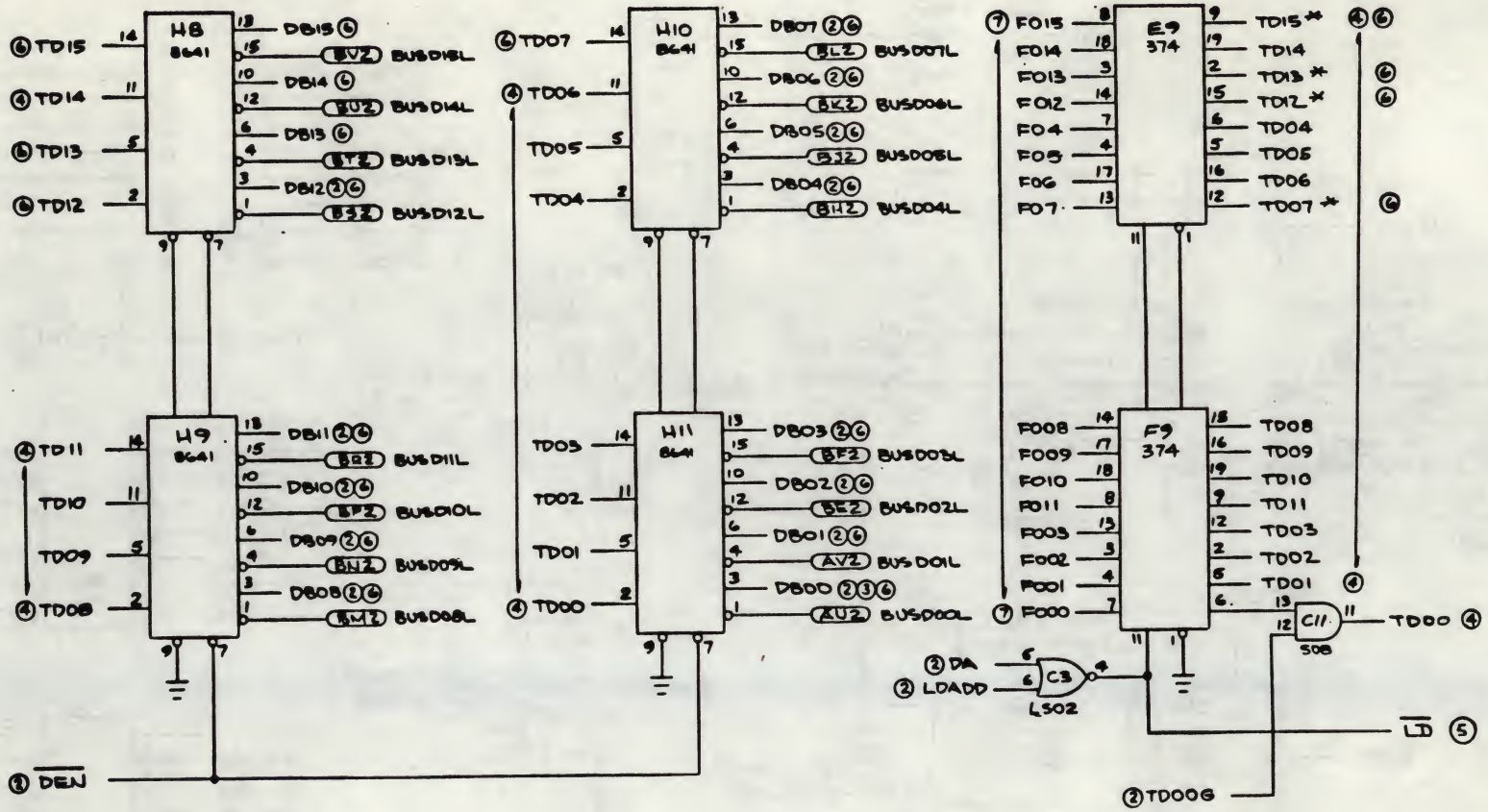


NOTE: SYMBOL ▷ INDICATES 16 PIN DIP CONNECTOR LOCATED AT H14

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 3 OF 13
		DRAWING NUMBER 853016 A



DATA BUS RCVR / DVR

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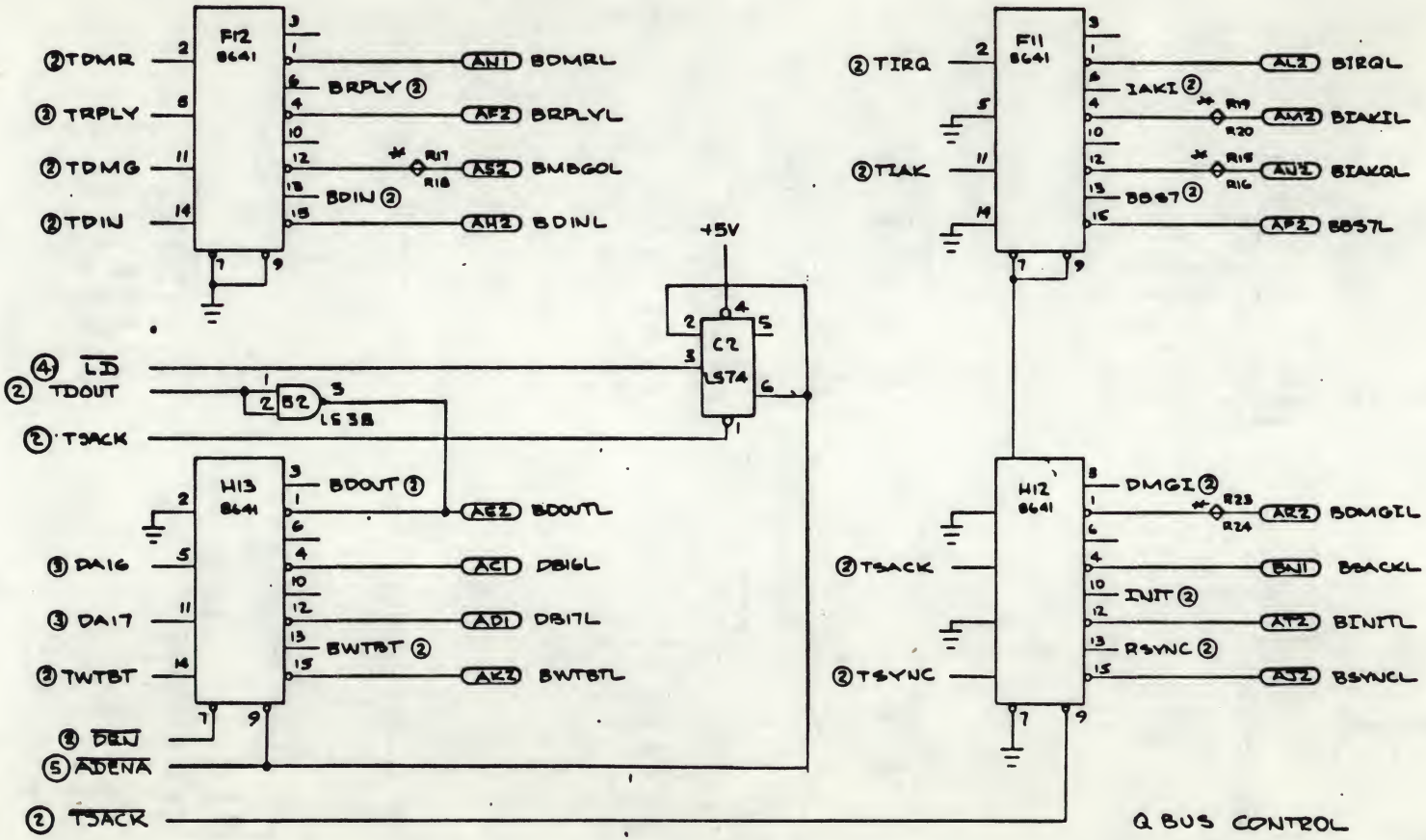
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 4 OF 13
		DRAWING NUMBER 853016 A



NOTE: SYMBOL * RX 180Ω / RX 390Ω INDICATES "PULL-UP" (180Ω), "PULL DOWN" (390Ω) RESISTORS.

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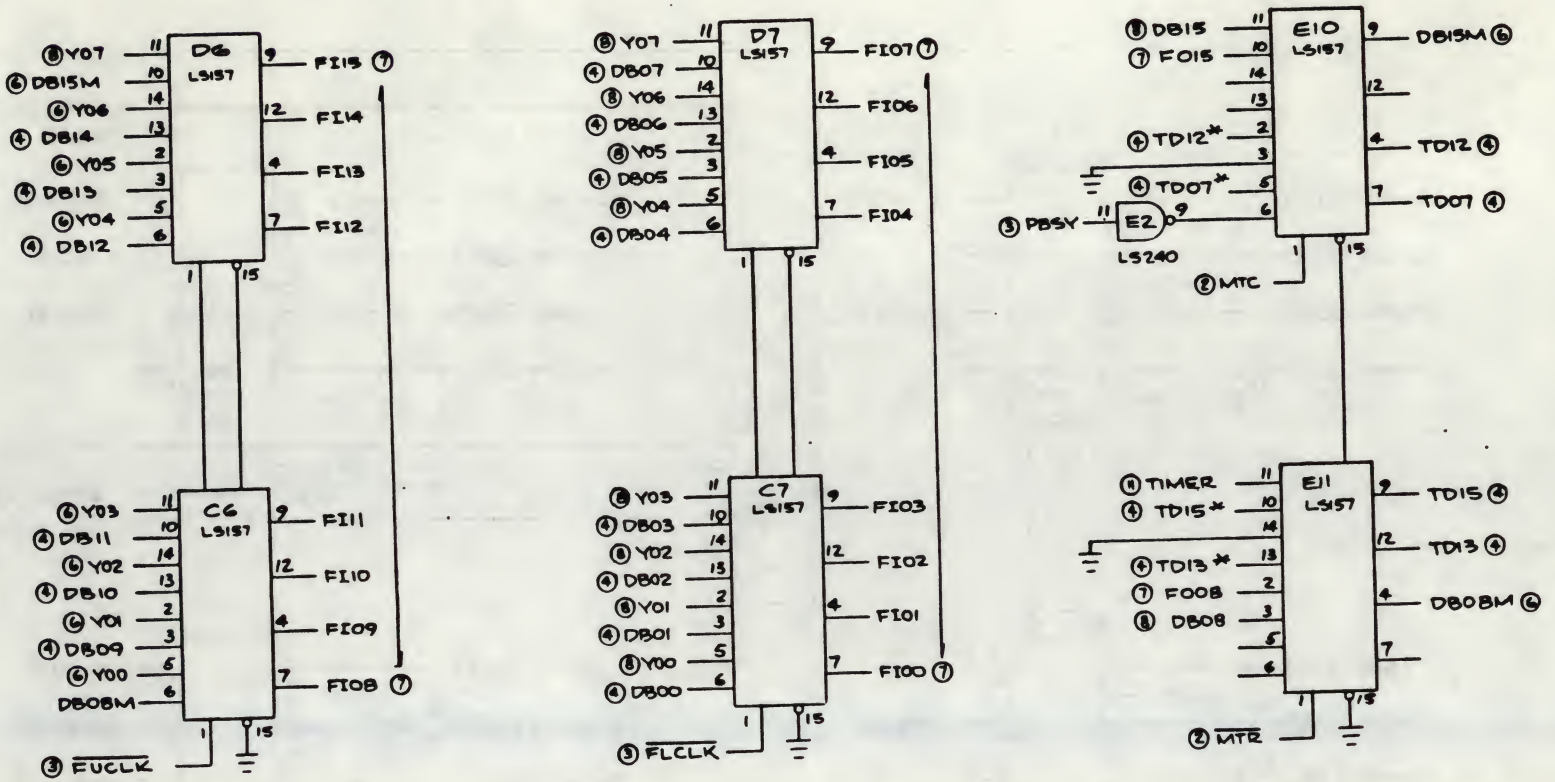
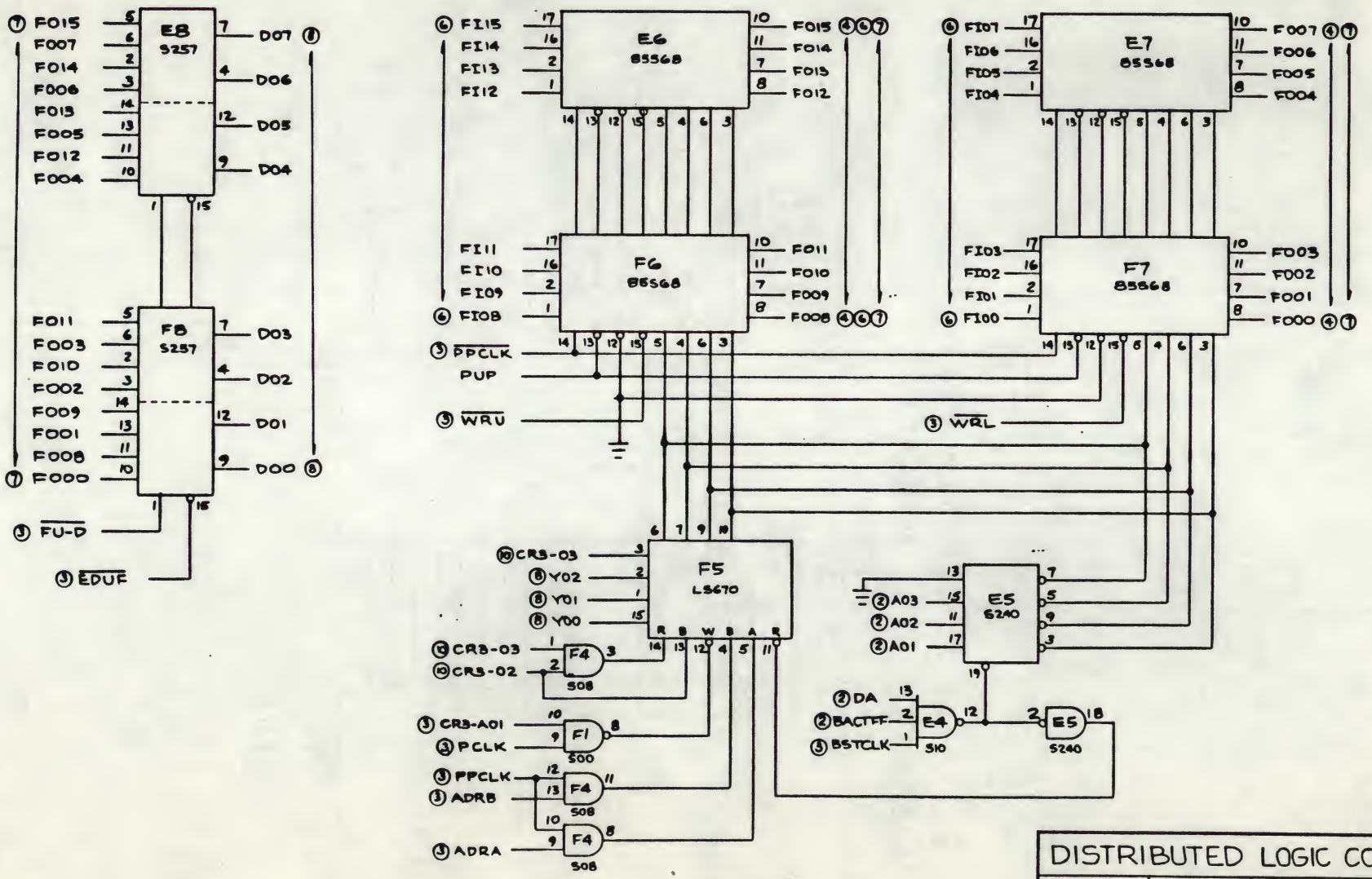
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 5 OF 13
		DRAWING NUMBER 853016 A



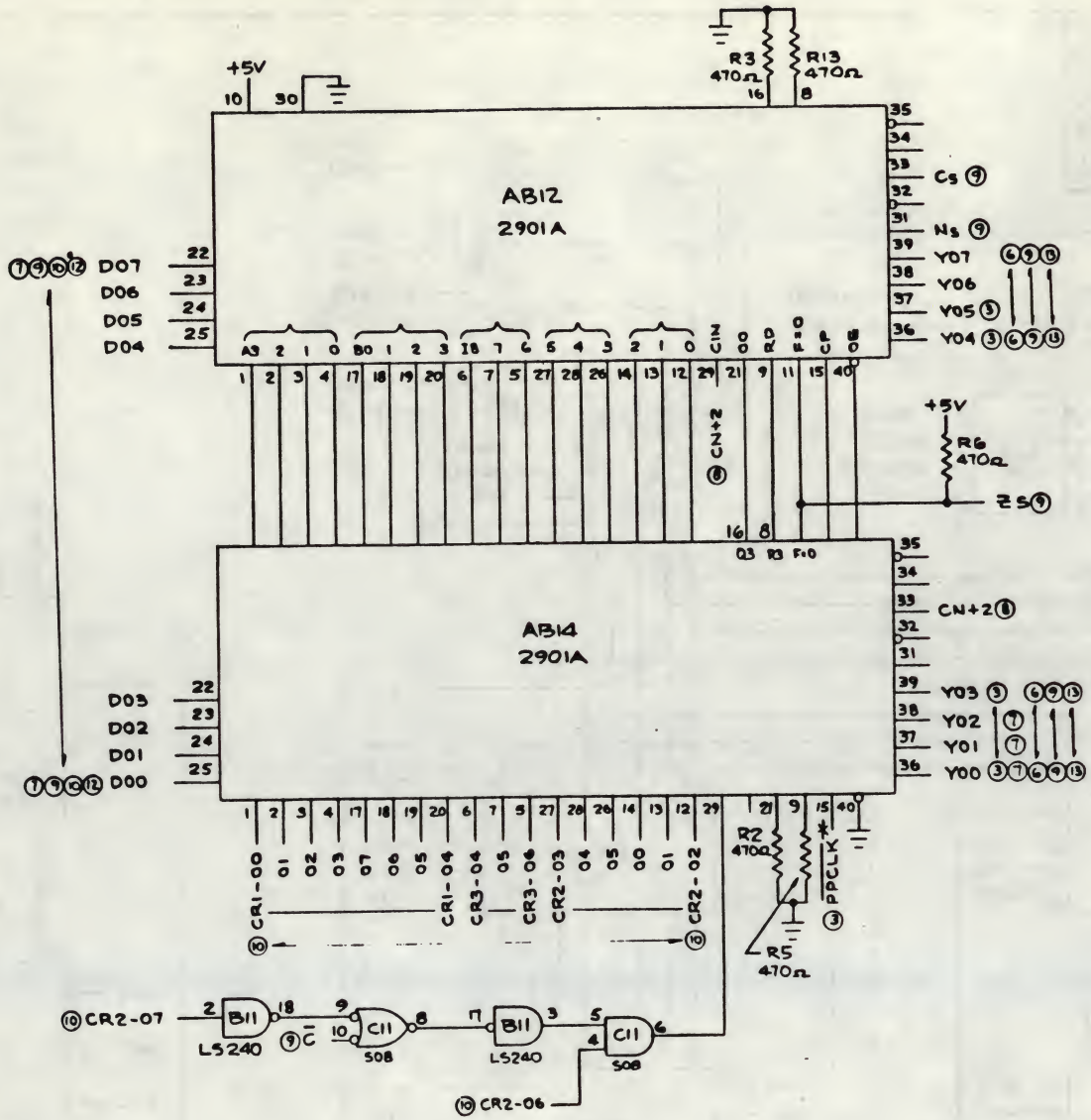
DATA FILE MUX

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 6 OF 13
		DRAWING NUMBER 853016



DATA FILE

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 7 OF 13
		DRAWING NUMBER 853016



1. RESISTORS ARE 470Ω ±5%, ¼W

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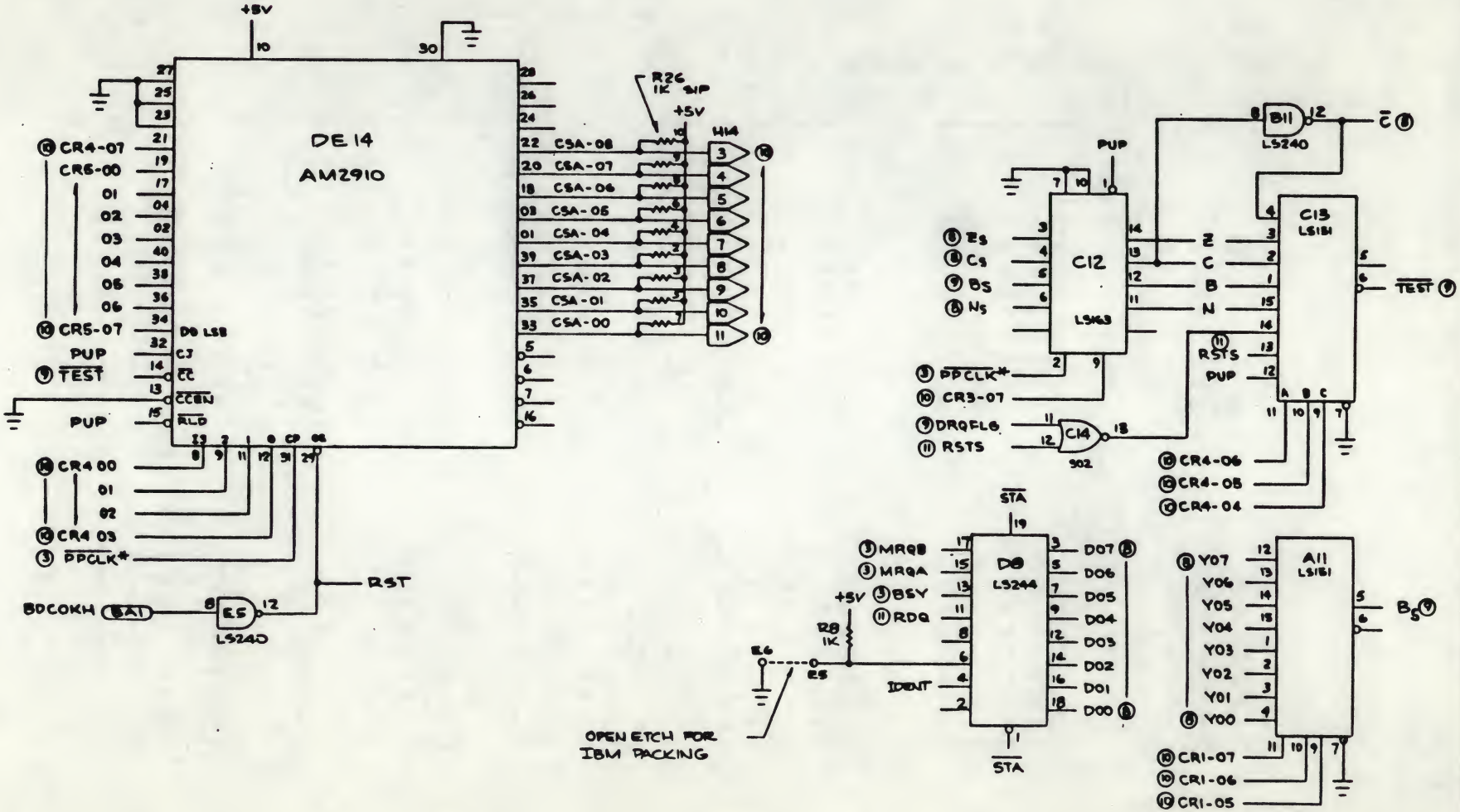
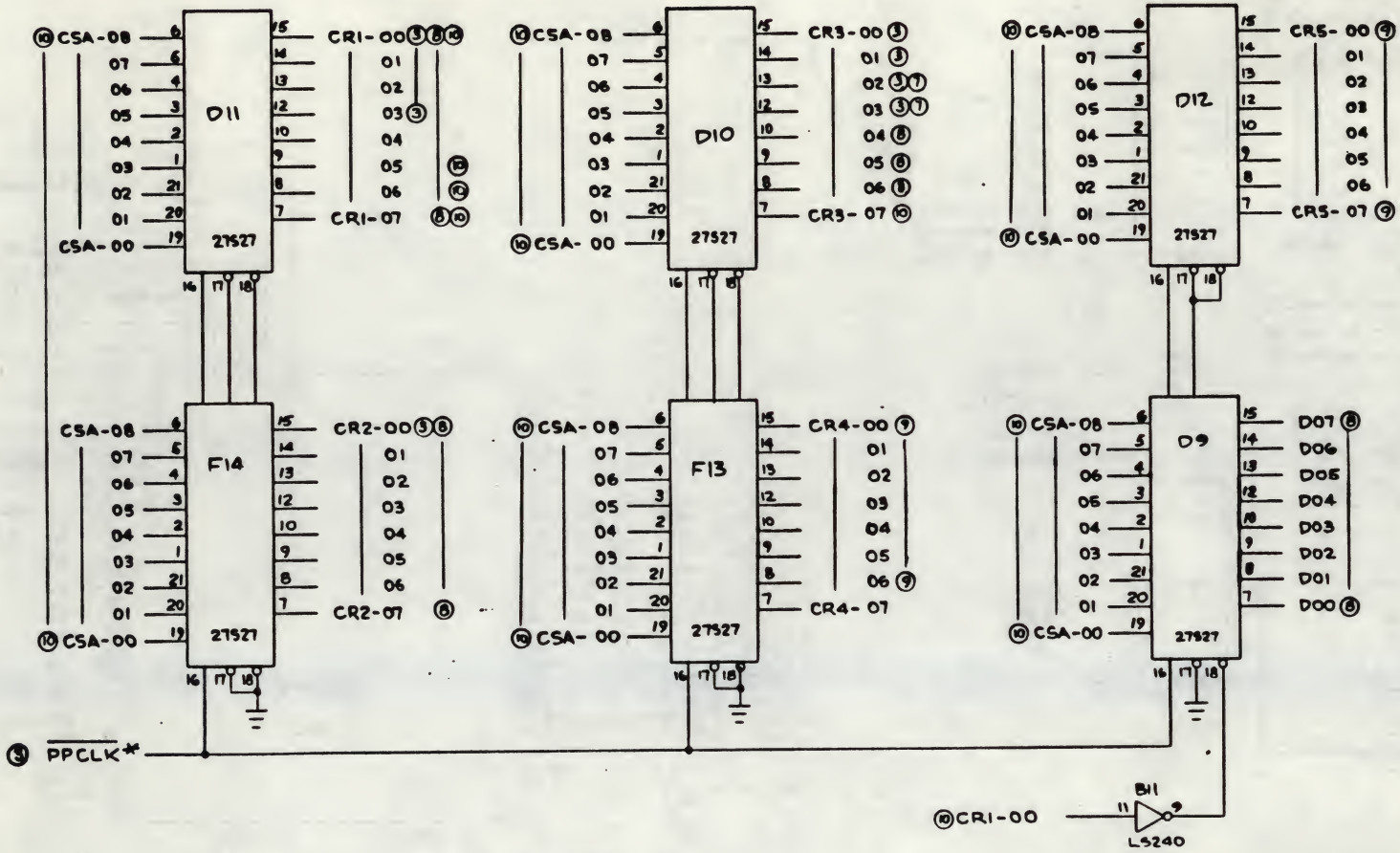
DATE		REVISED
LOGIC DIAGRAM, DQ130		SHT 8 OF 13
		DRAWING NUMBER 853016



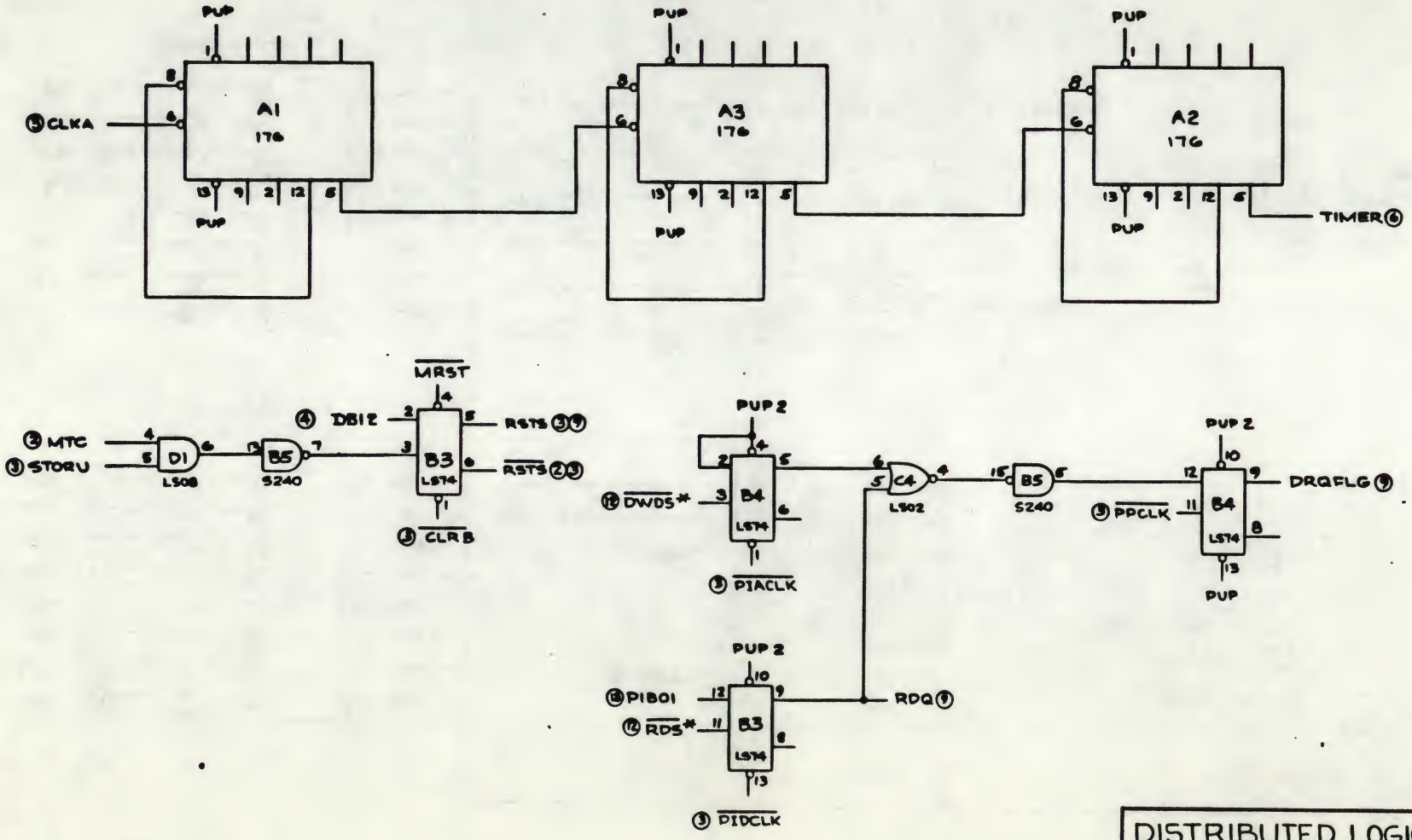
1. SYMBOL: (X) INDICATES 16 PIN "DIP" CONNECTOR LOCATED AT H14

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 9 OF 13
		DRAWING NUMBER 853016

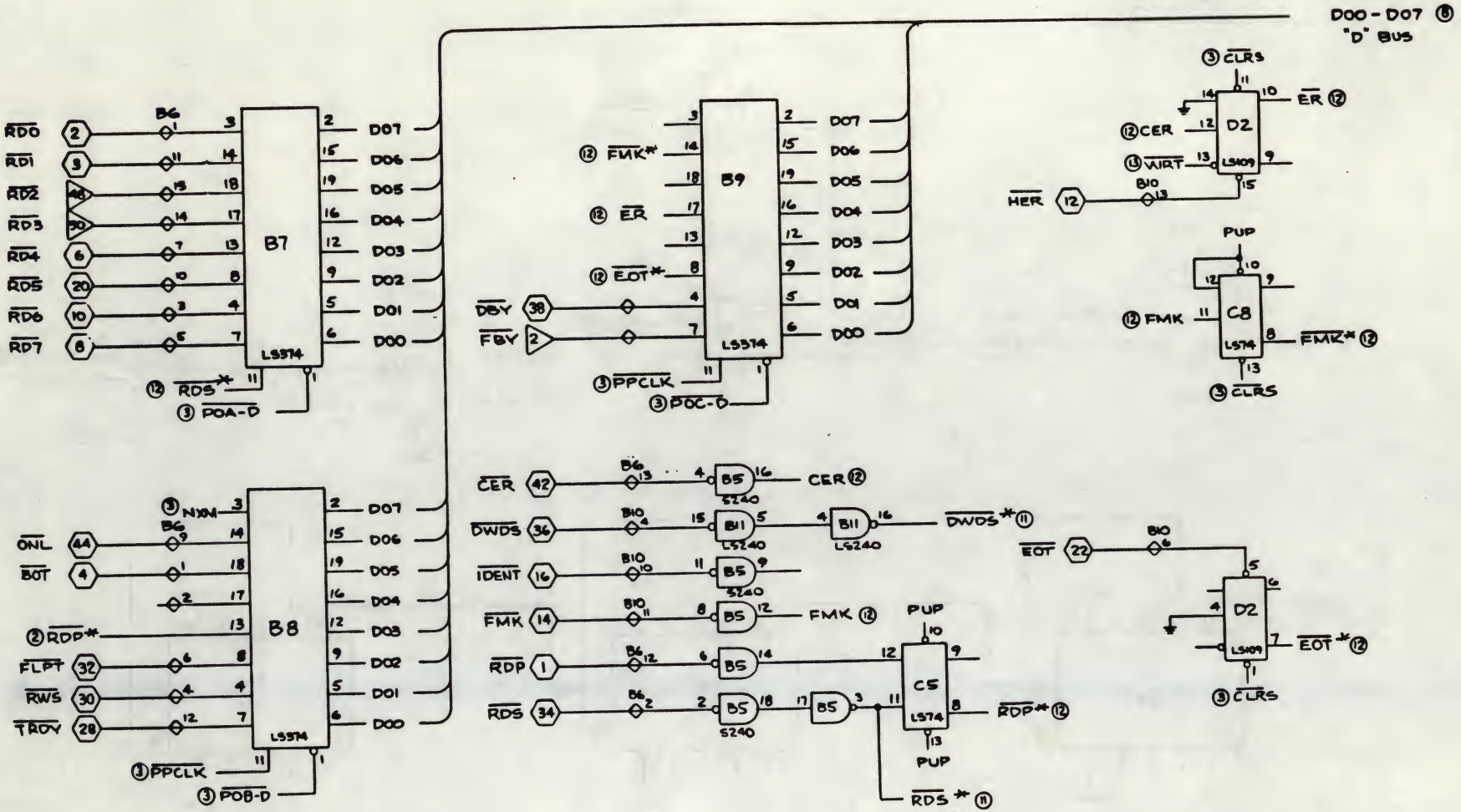


CONTROL STORE & PIPELINE

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 10 OF 13
		DRAWING NUMBER 853016



DISTRIBUTED LOGIC CORP.		
SCALE	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 11 OF 13
		DRAWING NUMBER 853016 A



SYMBOL ▷ INDICATES "J2", 50 PIN CONNECTOR (ALL ODD PINS ARE GND.)

SYMBOL ⬡ INDICATES "J1", 50 PIN CONNECTOR (ODD PINS EXCEPT 1 & 3 ARE GND.)

NOTE: SYMBOL —◇— INDICATES 220Ω/330Ω TERMINATOR

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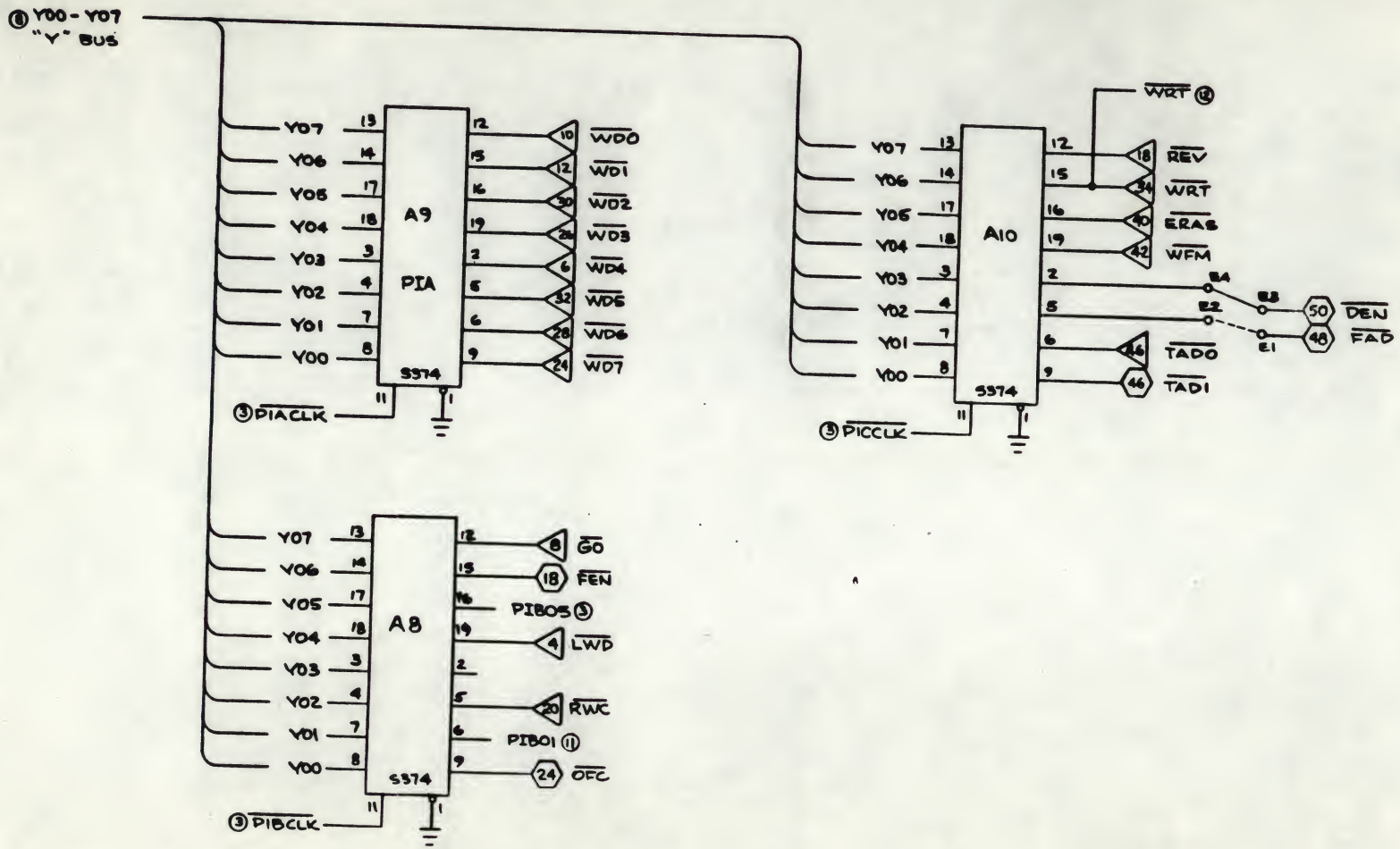
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 12 OF 13
		DRAWING NUMBER 853016



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM, DQ130		SHT 13 OF 13
		DRAWING NUMBER 853016 A